

Sapporo_GLK Schematics

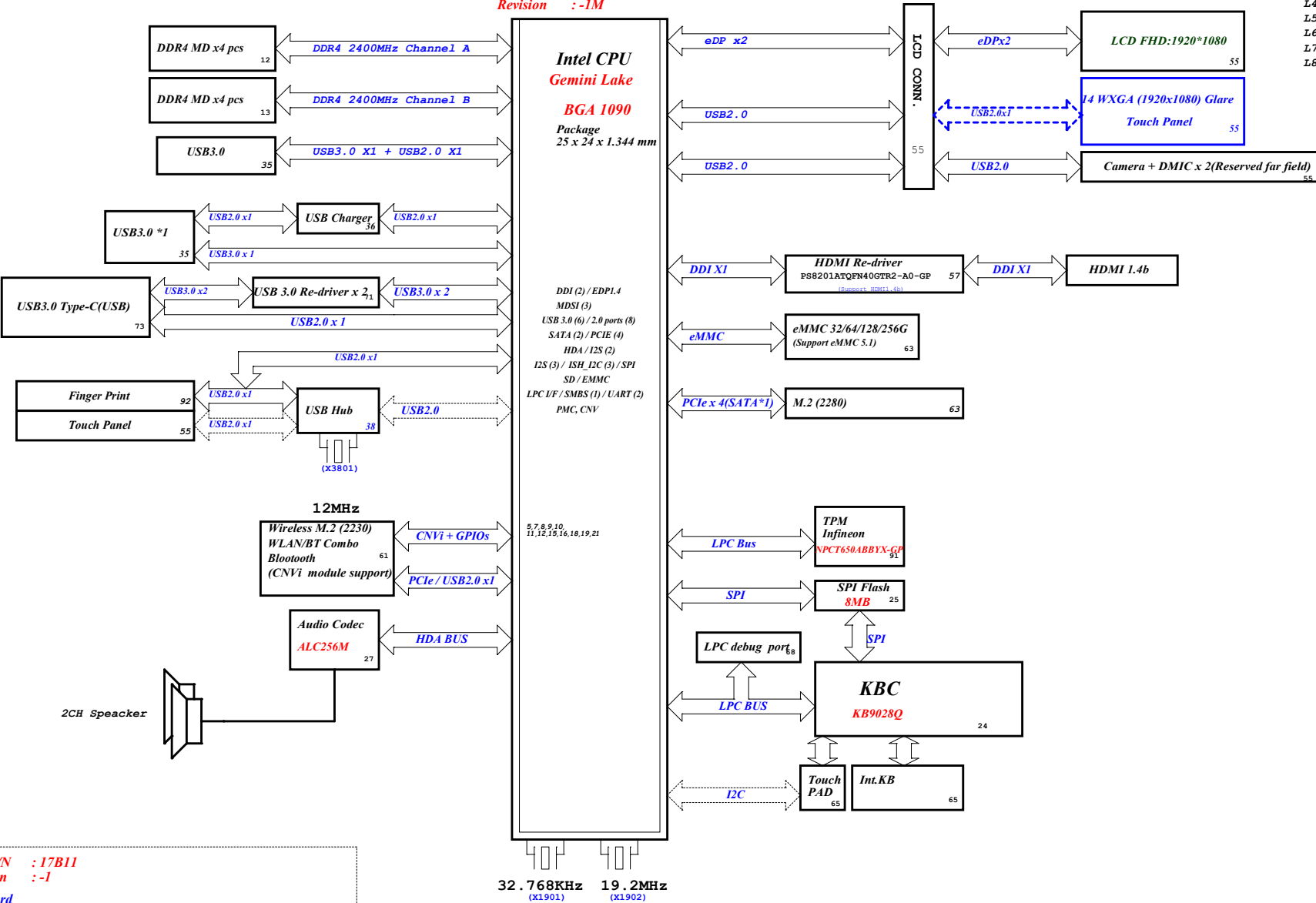
Gemini Lake

Gemini Lake Board Block Diagram

Project code : 4PD0E6010001
PCB P/N : 17891
Revision : -1M

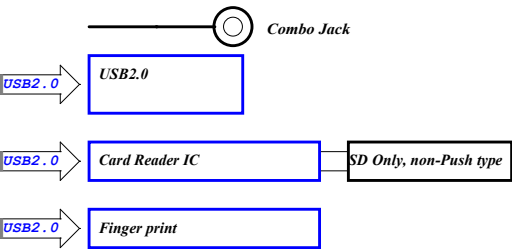
PCB Layer

- L1: Top
L2: GND
L3: Signal
L4: GND
L5: Signal
L6: Signal
L7: GND
L8: Bottom



CHARGER		44
BQ24780S		
INPUTS	OUTPUTS	
19V_DCBATOUT	BT+	
SYSTEM DC/DC		45
SY8288CRAC-GP		
INPUTS	OUTPUTS	
19V_DCBATOUT	5V_S5	
SYSTEM DC/DC		45
SY8288CRAC-GP		
INPUTS	OUTPUTS	
19V_DCBATOUT	3D3V_S5	
CPU PMIC		46
BD2671MWV-E2-GP		
INPUTS	OUTPUTS	
19V_DCBATOUT	1D8V_S5	
CPU PMIC		47
BD9515NUXE2-GP-U		
INPUTS	OUTPUTS	
5V_S5	1V_CPU_VCGI	
CPU PMIC		50
BD2671MWV-E2-GP		
INPUTS	OUTPUTS	
5V_S5	1V_CPU_VNN	
	1D05V_S0	
CPU PMIC		51
BD2671MWV-E2-GP		
INPUTS	OUTPUTS	
19V_DCBATOUT	1D2V_CPU_VDDQ_S3	
5V_S5	1D2V_S5	
	2D5V_S3	
SYSTEM Load switch		40
G2898KD1U		
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
1D8V_S5	1D8V_S0	

PCB P/N : 17B11
Revision : -1
IO Board



4GB No eMMC

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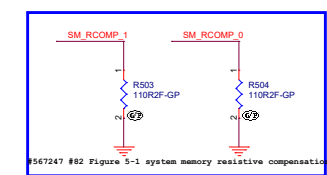
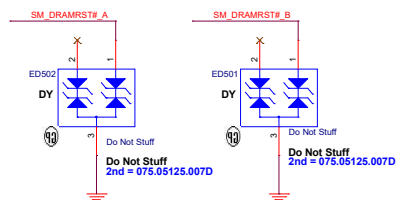
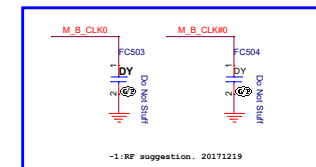
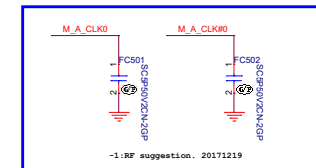
12 M_A_DQ[63:0] <<
12 M_A_A[16:0] <<
12 M_A_DQS_DN7[0] <<
12 M_A_DQS_DP7[0] <<

12 M_A_CS0 <<
12 M_A_CLK0 <<
12 M_A_CKE0 <<
12 M_A_BA1 <<
12 M_A_BA0 <<
12 M_A_BGN <<
12 M_A_ACT_N <<

12 V_SM_VREF_CNTA <<
12 SM_DRAMRSTB_A <<
12 SM_DRAMRSTB_B <<
12 V_SM_VREF_CNTB <<

13 M_B_DQ[63:0] <<
13 M_B_A[16:0] <<
M_B_DQS_DN7[0] <<
M_B_DQS_DP7[0] <<
13 M_B_CLK0 <<
13 M_B_CKE0 <<
13 M_B_CS0 <<
13 M_B_BA0 <<
13 M_B_BA1 <<
13 M_B_BA2 <<
13 M_B_BA3 <<

```



MEM_CH1_LCKE) AY29 SM_RCOMP_0

MEM_CH0_RCOMP BC15 SM_DRAMRST# B

MEM_CH1 RESET# RCOMP SM_RCOMP_1

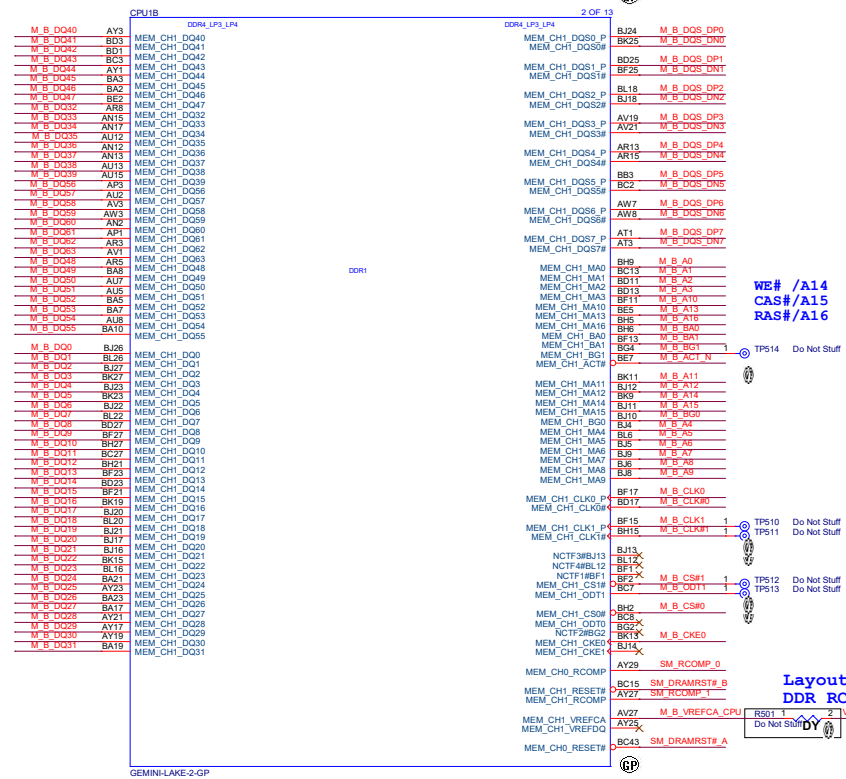
MEM_CH1_VREFCA AV27 M_B_VREFCA_CPU

MEM_CH1_VREFDQ AY25 R501 1 2 V_S_VREF_CNTB

MEM_CH0_RESET# BC43 SM_DRAMRST# A

Do Not Solder

DDR RCOMP trace

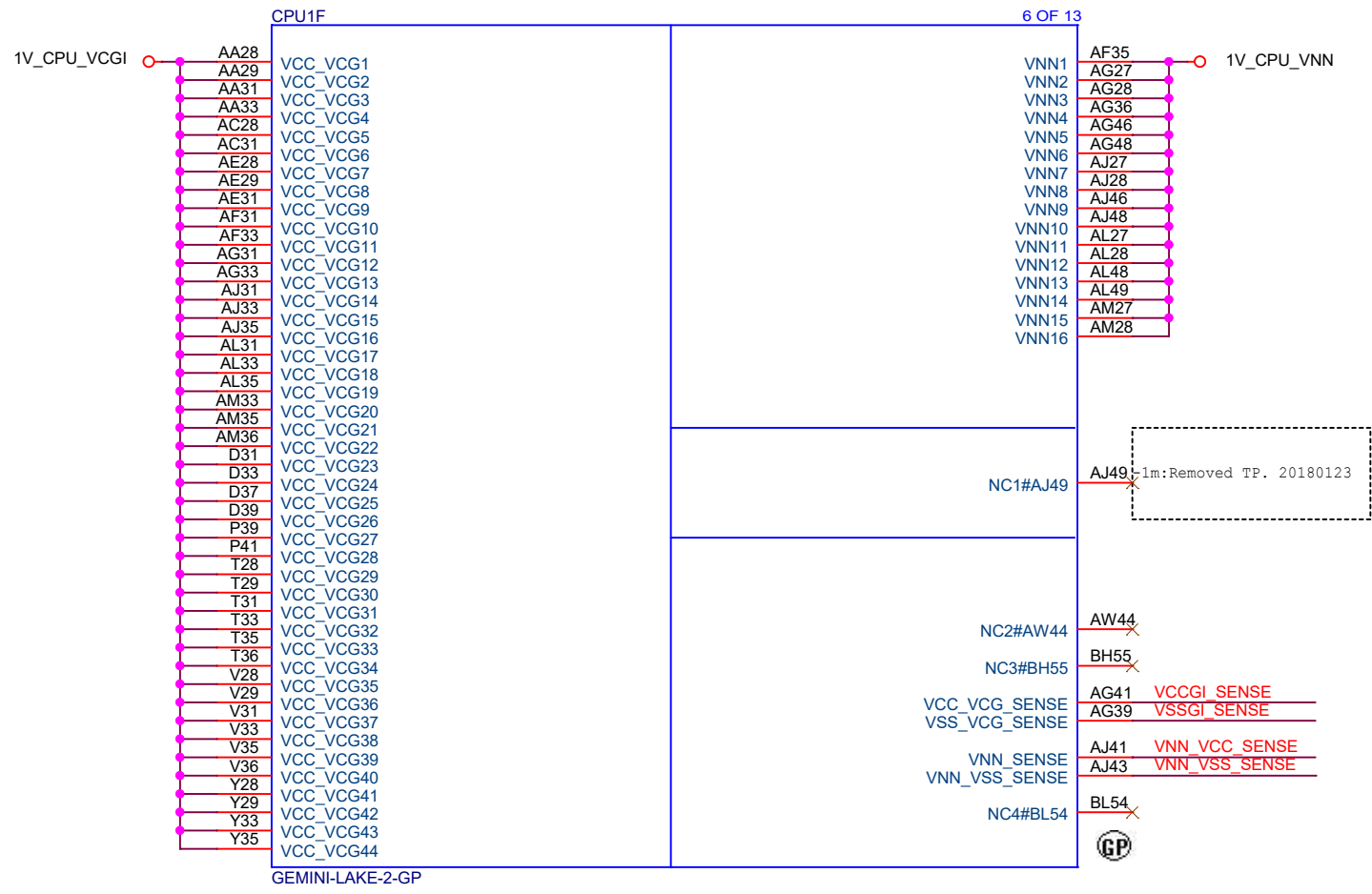


47 VSSGI_SENSE <<=====

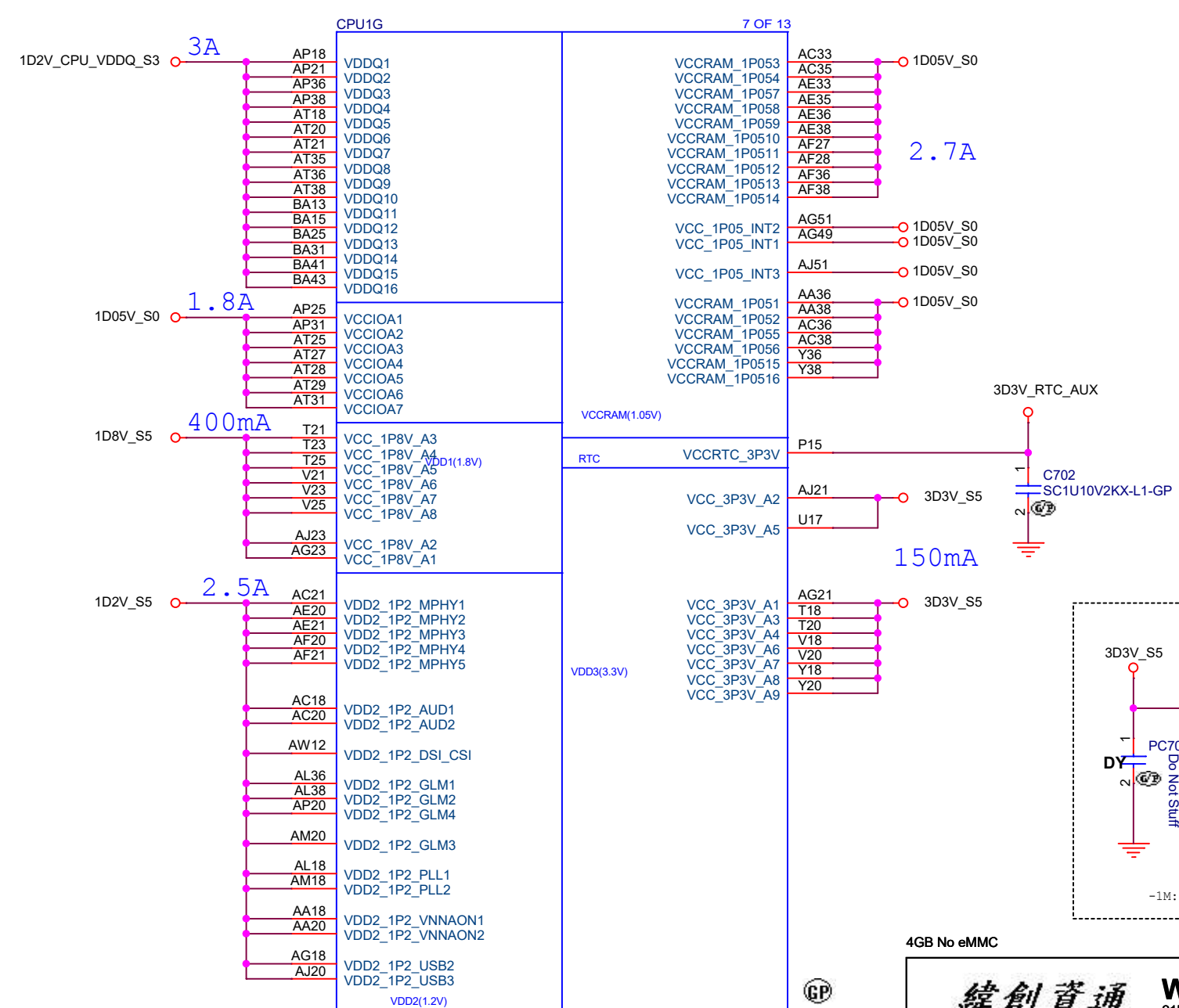
47 VCCGI_SENSE <<=====

50 VNN_VCC_SENSE <<=====

50 VNN_VSS_SENSE <<=====



SSID = CPU



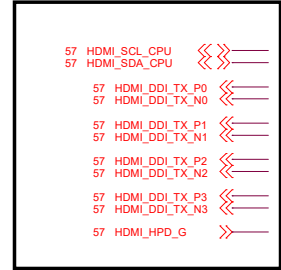
GEMINI-LAKE-2-GP
@ Tie VCCIOA to VDDQ for LPDDR4 designs
@ Tie VCCIOA to VCCRAM_1P05 for DDR4 designs

4GB No eMMC

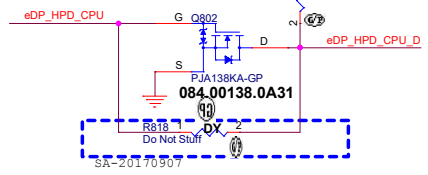
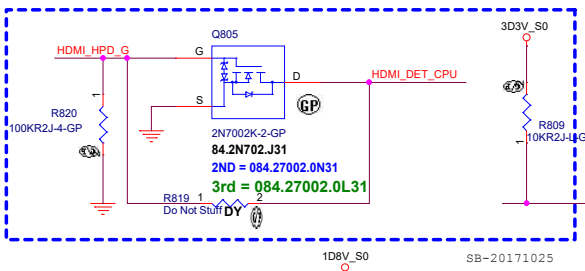
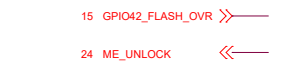
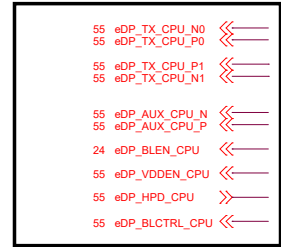
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (VDDQ/VCCIO/Others)			
Size: A4	Document Number: Sapporo_GLK		Rev: -1M
Date: Tuesday, February 13, 2018		Sheet: 7	of 106

SSID = CPU

HDMI



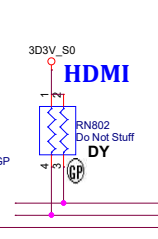
EDP



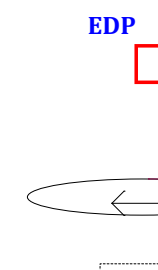
HV_DD10_HPD
It is required to enable internal 20k pull up resistor on the HV_DD12_HPD signals by BIOS.

Offset from 0x48	Bits	Default Value	Description	Usage	FIT Visible
36	170		GPIO_134 (vccio_pad_gpio_134): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
35	171		HV_EDP_HPD (vccio_pad_hv_edp_hpd): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default)		Yes
34	170		HV_DD11_HPD (vccio_pad_hv_ddi1_hpd): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
33	170		HV_DD10_HPD (vccio_pad_hv_ddi0_hpd): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
32	171		PANEL0_BKLTCTL (vccio_pad_panel0_bkltctl): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default)		Yes
31	171		PANEL0_BKLTEN (vccio_pad_panel0_bkltten): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default)		Yes
30	171		PANEL0_VDDEN (vccio_pad_panel0_vdden): 0 = PAD VCCIO is 3.3V 1 = PAD VCCIO is 1.8V (default)		Yes
29	170		HV_DD11_DDC_SCL (vccio_pad_hv_ddi1_ddc_scl): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
28	170		HV_DD11_DDC_SDA (vccio_pad_hv_ddi1_ddc_sda): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
27	170		HV_DD10_DDC_SCL (vccio_pad_hv_ddi0_ddc_scl): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes
26	170		HV_DD10_DDC_SDA (vccio_pad_hv_ddi0_ddc_sda): 0 = PAD VCCIO is 3.3V (default) 1 = PAD VCCIO is 1.8V		Yes

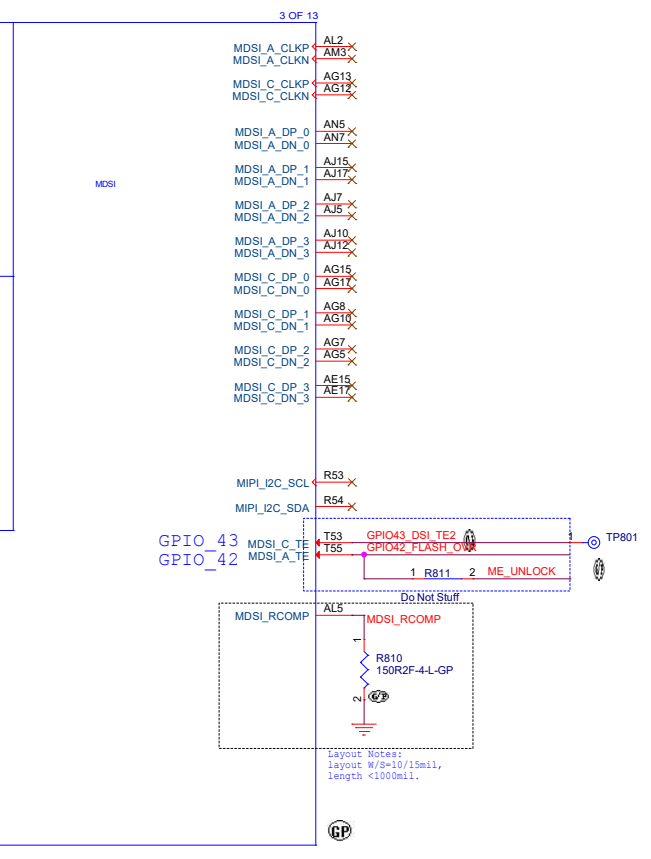
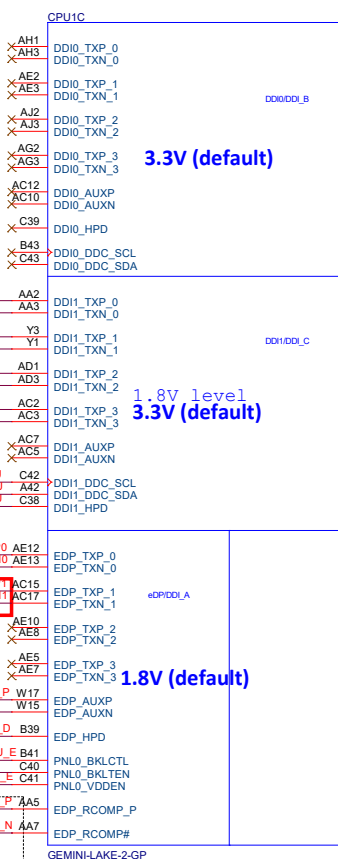
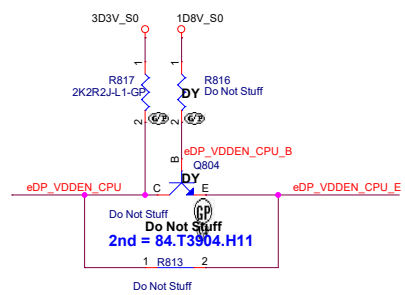
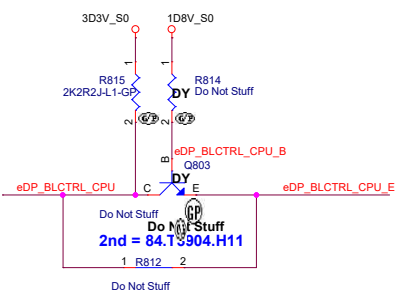
HDMI



EDP



Impedance 85 Ohm and space 20mil, length <400mil.



15.1.2.SHPD Implementation
The hot-plug detect output from eDP* sink device is a 3.3V active high signal. Since the input on the processor is a 3.3V active low signal, a logic inversion circuit is required on the motherboard. Figure 15-7 shows an example of this implementation.

4GB No eMMC

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CPU (DDI/EDP/MDSI)

Sapporo GLK

1M

Tuesday, February 13, 2018

8 of 106

SSID = CPU



4GB No eMMC

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VSS)

Size

Document Number

Rev

Sapporo GLK

-1M

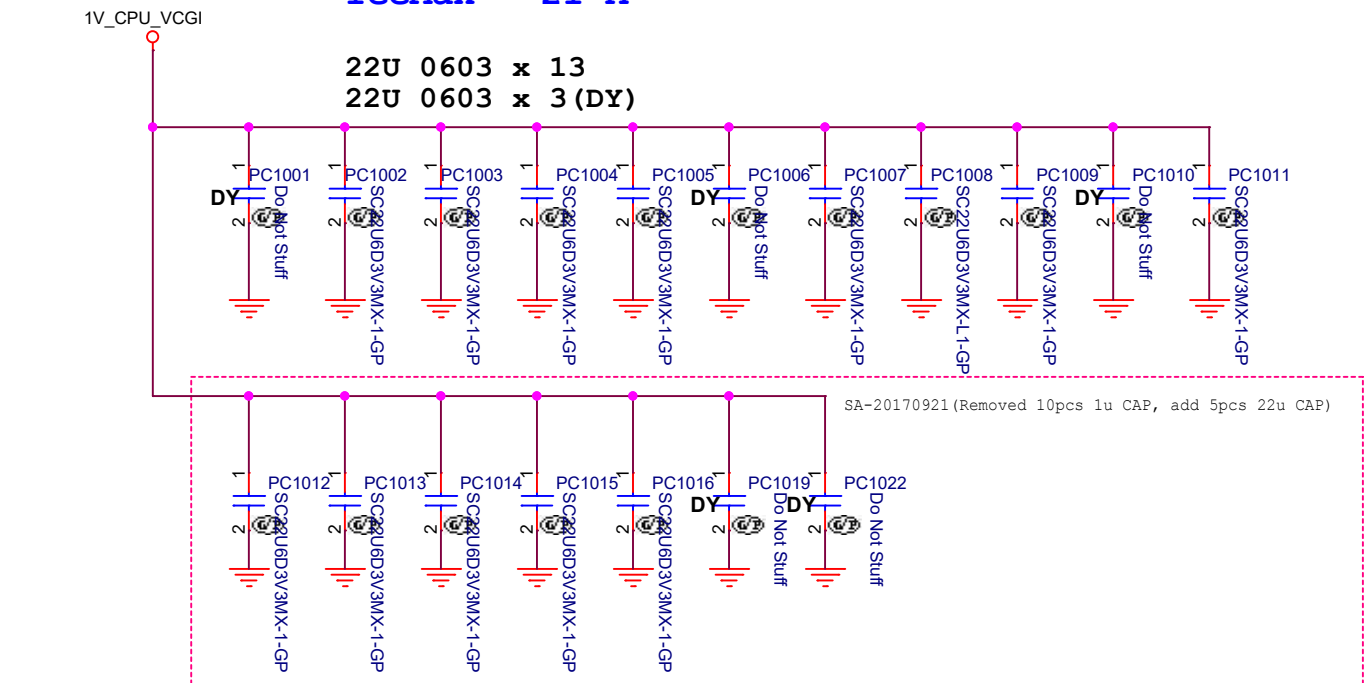
Date: Tuesday, February 13, 2018

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SSID = CPU

VCCGI
IccMax = 21 A

22U 0603 x 13
22U 0603 x 3 (DY)



VNN

22U 0603 x 6
22U 0603 x 2 (DY)

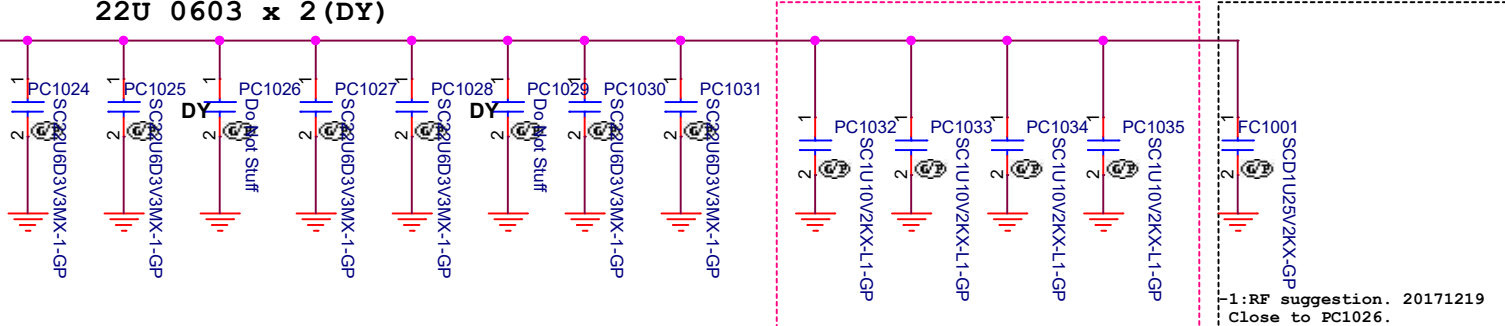


Table 4-3. Decoupling Requirements of BSC, ESC, MLCC, Bulk Cap and SoC Ball Groups (Sheet 1 of 2)

System Rail Name	Power Balls [GND]	Max L from Ball to nearest BSC [0402-1uF]			Max L from Ball to nearest ESC [0402 - 1uF]			Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF]			Max L / R from Ball to VR Bulk [330uF_9mOhm]		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCC_VCG I	T28,T29,T31,T33,T35,T36, V28,V29,V31,V33,V35,V36, Y28,Y29,Y33,Y35,AA28,AA29,A A31,AA33,C28,AC31,AE28,E29, AE31,F31,AF33,AG31,AG33,AJ 31,AJ33,AJ35,AL31,AL33,AL35, AM33,AM35,AM36,D33,D39,D3 1,P41,P39,D37 [AM38,AG38,Y27,AA27,AC27,A F29,AG29,AJ29,AL29,AM29,AM 31,AP29,V27,T27,R28,Y31,AG3 5,AJ36,AA35,AC29,V38,T38,C3 6,E28,F31,H39,E27,AP33,AP35 ,M41, AL39,N28,D41]	C414 C410 C422 C440 C420 C411 C407 C425 C441 C416 C426 C421	1.3 0.875 1.1 0.654 0.496 0.452 0.602 0.688 0.405 0.387 0.417 0.386	0.103				C612 C613 C614 C615 C616 C617 C618	0.424 0.418 0.425 0.409 0.406 0.437 0.420	0.226	C702 C703	0.410 0.415	1.41 1.41
VNN-SVID	AF35,G36,G27,AG28,AJ27,AJ2 8,AL27,AL28,AJ48,AL48,AL49,A J46,AG46,AG48,AM28,AM27 [AF29,AG29,AJ29,AL29,AM29,A P27,AP28,AP29,AF25,AG25,AJ2 5,AL25,AM25,AG35,AJ36,AG38 ,AL46,AN48,AN49,AJ44,AF45,A F47,AF48,AL51]	C431 C401 C419 C430	0.565 0.652 0.435 0.434	0.332				C605 C606 C604	1.68 1.78 1.75	1.519			

4GB No eMMC

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Title

CPU (Power CAP1)

Size

A4

Document Number

Sapporo_GLK

Rev

-1M

Date

Tuesday, February 13, 2018

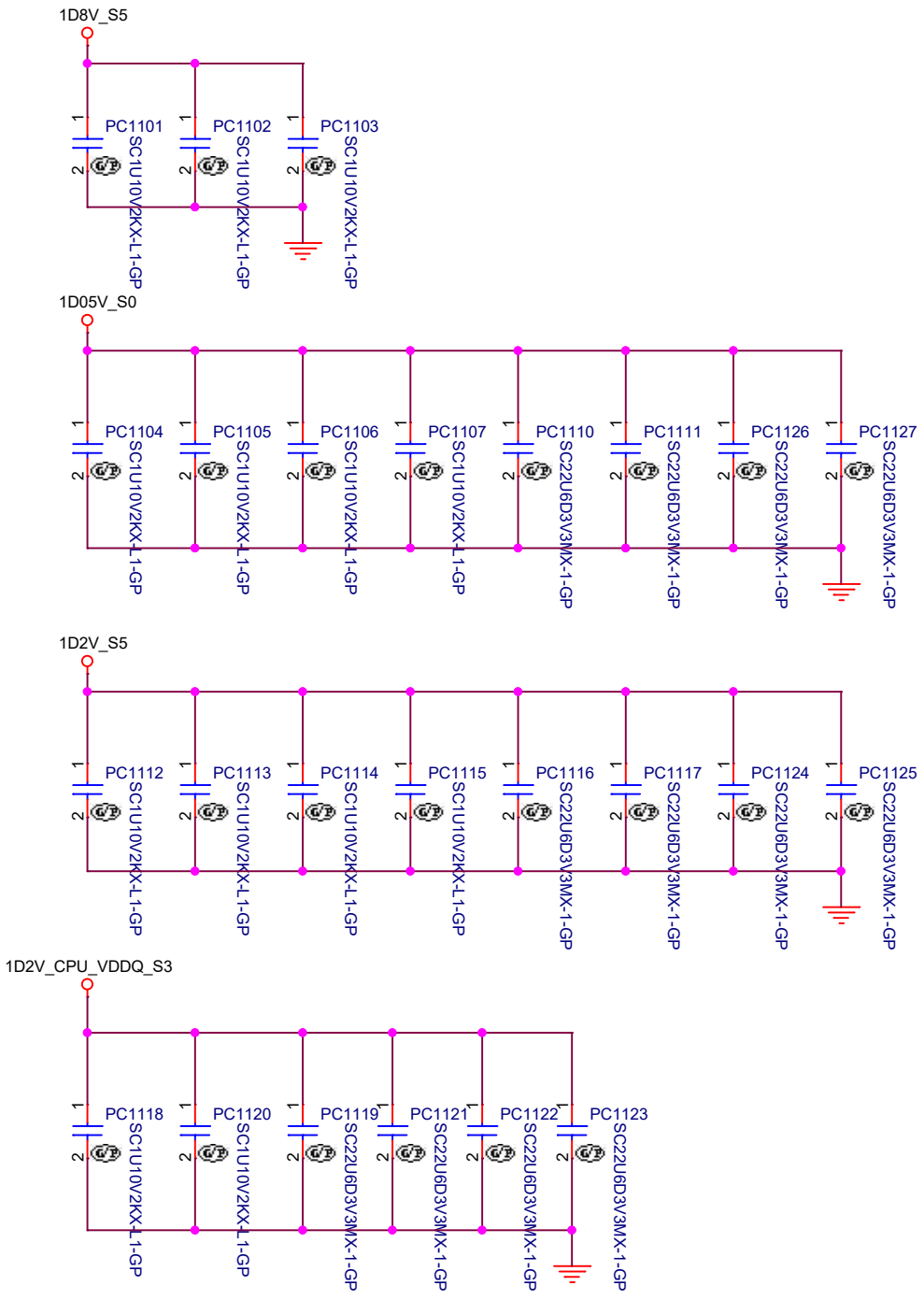
Sheet

10

of

106

SSID = CPU



System Rail Name	Power Balls [GND]	Max L from Ball to nearest BSC [0402-1uF]			Max L from Ball to nearest ESC [0402 - 1uF]			Max L from Ball to nearest MLCC [0603 - 22uF *0805 - 22uF #0805 - 47uF]			Max L / R from Ball to VR Bulk [330uF_9mOhm]		
		Back Side Cap	BSC (nH)	Total (nH)	Top Side Edge Cap	ESC (nH)	Total (nH)	Top Side MLCC	MLCC (nH)	Total (nH)	Top Side Bulk	Bulk (nH)	(mΩ)
VCC_1P8V_A	V21,T25,V25,T23,V23,T21 [Y27,Y25,Y23,Y21,T27,V27,P21] AJ23,AG23[AJ25, AG25]	C417 C438 BSC_U SB	1.36 0.714 1.29	0.673									
VCCIOA	AT27,AT28,AT29,AT25,AP31,AT31,AP25 [AM29,AP27,AP28,AP28,AP33,AT33,AP23,AT23,AU28,AM31]	C429 C418	0.475 0.475	0.426	C202 C203	3.72 4.10	3.6	C601 C602	5.12 4.78	4.537			
VDDQ	AP36,AT36,AP38,AT38,AT35,AT18,AP18,AP21,AT20,AT21,BA43,BA41,BA31,BA13,BA15,BA25 [AV39,AR39,AP35,AM38,AT33,AP33,AT23,AR17,AP23,AM23,AM21,AY43,AV33,BC31,AV23,AV17,AV41,AY41,BC25,AY13,AY15]	C412 C428	0.475 0.523	0.223				*C816 *C817 *C820 *C821	2.06 4.10 1.62 3.30	0.496			
VCCRAM_1P05	AC35,AE35,AE38,AE36,AF28,AF27,AF38,AF36,AC33,AE33 [AE27,AF29,AF40,AG38,AJ38,AC29,AA35,AG35,AJ36,AF25]	C424	0.712					C608	2.89				
VCCRAM_1P05_10	AA36,AA38,Y36,Y38,AC38,AC36 [V38,W39,AF40,W41,T38,AA35]	C405	0.989					C609	3.62				
VDD2_1P 24_GLM	AP20,AL38,AL36 [AM21,AR17,AJ38, AJ36]	C415	0.619		C219	1.78		C610 C611	2.10 2.09	1.978			
VDD2_1P 24_AUD_I SH_PLL	AM18,AL18 [AJ18, AL17]	C435	0.791					#C823 #C824	1.88 1.88	1.75			
VDD2_1P 24_USB2	AJ20,AG18 [AG20, AJ18]	C433	0.747		C217	1.723		C623	2.13				
VDD2_1P 24_MPHY	AC21,AE20,AE21,AF20,AF21 [AG20,AF18,AE18,AA23,AC23,AE23,AF23,AA21]	C442	0.667		C218	1.6		C624	2.08				
VDD2_1P 24_DSI_C SI	AW12[AW10]							C625	2.22				

4GB No eMMC

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Title

CPU (Power CAP2)

Size A4

Document Number

Sapporo_GLK

Rev -1M

Date: Tuesday, February 13, 2018

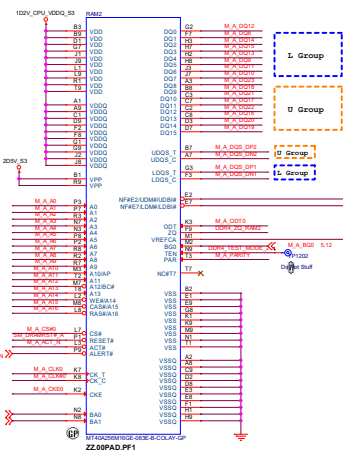
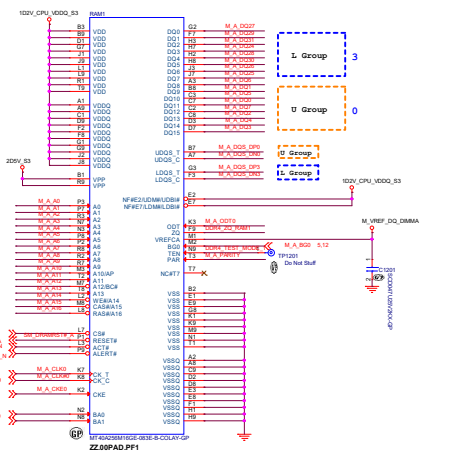
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Main Func = DDR4 On Board With Single Rank

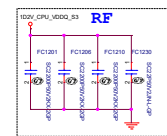
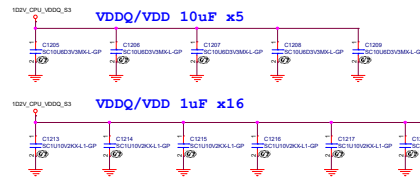
DQ80	DQ0~DQ7
DQ81	DQ8~DQ15
DQ82	DQ16~DQ23
DQ83	DQ24~DQ31
DQ84	DQ32~DQ39
DQ85	DQ40~DQ47
DQ86	DQ48~DQ55
DQ87	DQ56~DQ63

5 M_A_DQ80-81
5 M_A_DQ82-83
5 M_A_DQ84-85
5 M_A_DQ86-87

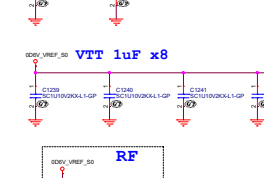
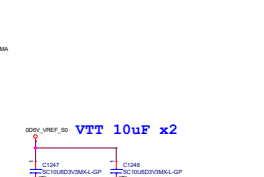
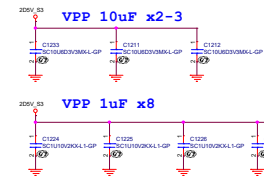
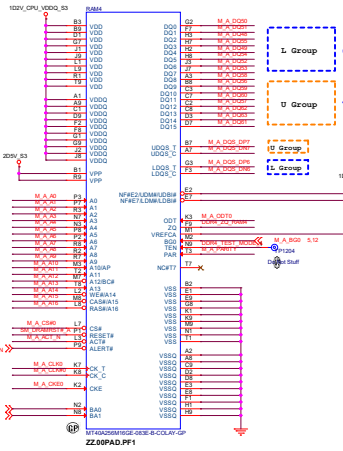
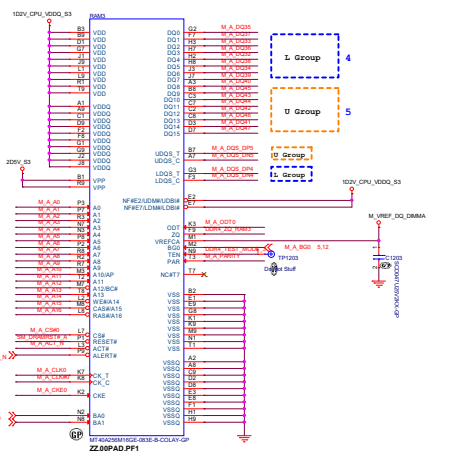
5 M_A_DQ88-89
5 M_A_DQ90-91
5 M_A_DQ92-93
5 M_A_DQ94-95
5 M_A_DQ96-97



DDR4 On Board RAM Power Decouple Cap



RF



5.6.4.3 Routing Guidelines for DQ Signals

DQ Signals pins from Soc MEM_CH0, DQ010, MEM_CH0, DQ011 and MEM_CH1, DQ010, MEM_CH1, DQ011 are unconnected

DRAM DQ Pins are connected to Ground Refer Figure 5-15

Figure 5-15. DQ Signal Connection Diagram

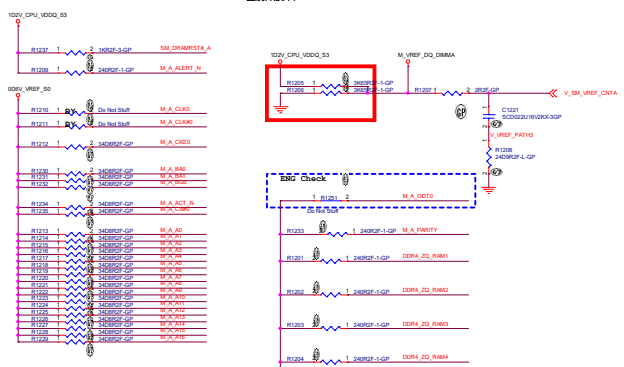
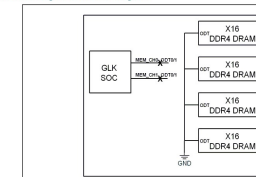
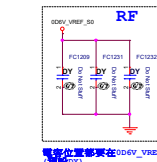
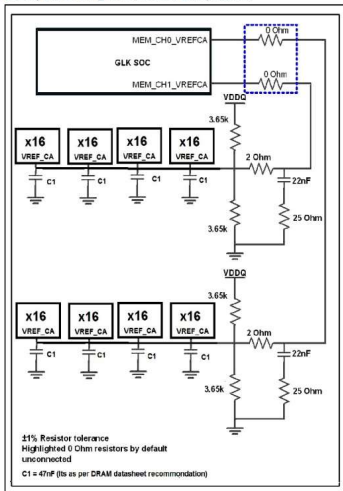


Figure 5-14. Memory Down DRAM_VREF Generation Example Circuit



RF

Table 5-14. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1uF (0402)	2
		Distribute evenly across domain, close by Drams	10x 10uF (0603)	
	Vpp	2 as near each x16 DRAM device as possible	16x 1uF (0402)	2
		Distribute evenly across domain, close by Drams	5x 10uF (0603)	2
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402)	2
		Distribute evenly across domain, close by Drams	4x 10uF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be dependent on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.

[561280] 4.23.5 XRL-U DDR4 Memory Down Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uF (size)
DDR4 Memory Down x16 = 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1uF (0402) (A11 stuffed)
		Distributed around the DRAM device	10x 10uF (0603) (A11 stuffed)
	Vpp	2 as near each x16 DRAM device as possible	16x 1uF (0402)
		Distributed around the DRAM device	5x 10uF (0603)
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402)
		Distributed around the DRAM device	4x 10uF (0603)

DQ80	DQ0-DQ7
DQ81	DQ8-DQ15
DQ82	DQ16-DQ23
DQ83	DQ24-DQ31
DQ84	DQ32-DQ39
DQ85	DQ40-DQ47
DQ86	DQ48-DQ55
DQ87	DQ56-DQ63

- 5 M_B_DQ80/81
- 5 M_B_A0/82
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
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- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

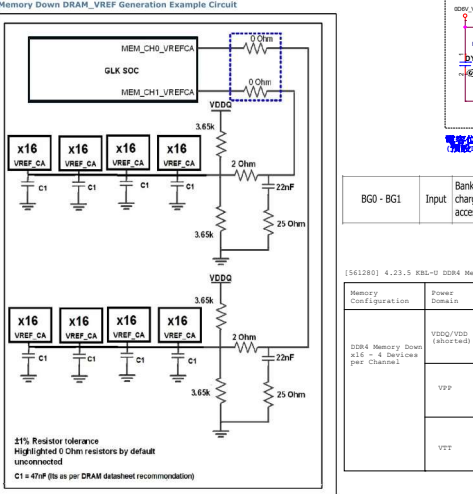
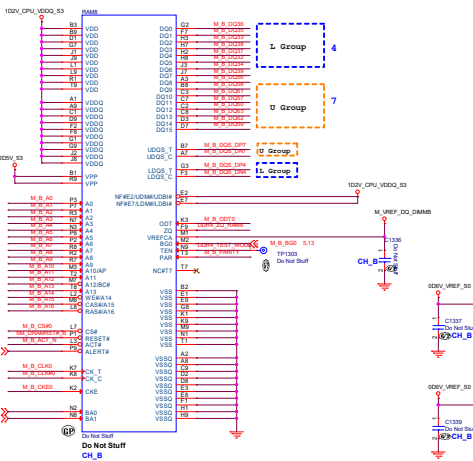
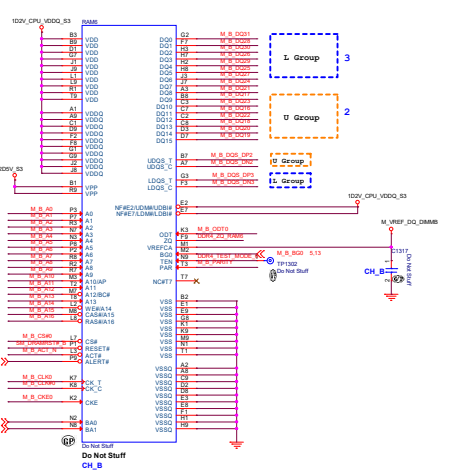
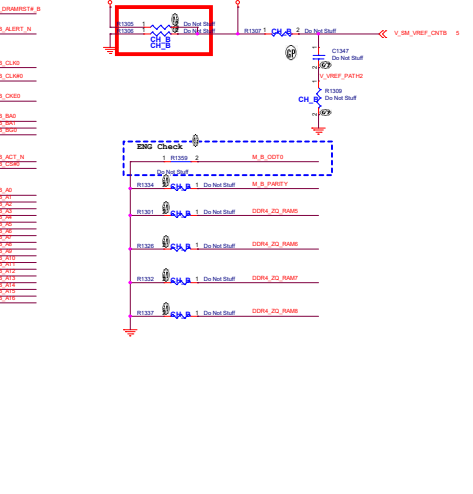
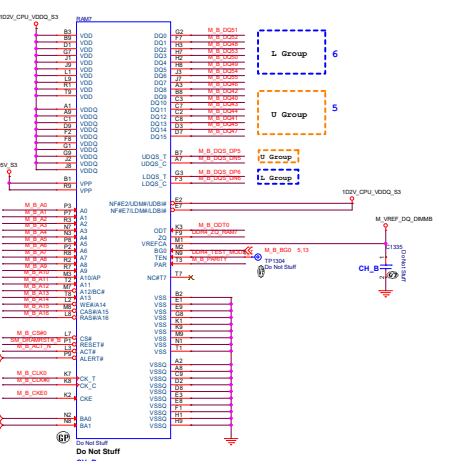
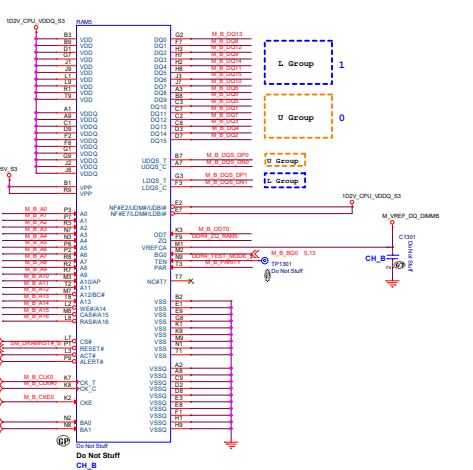
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- 5 M_B_ACT_N
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- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

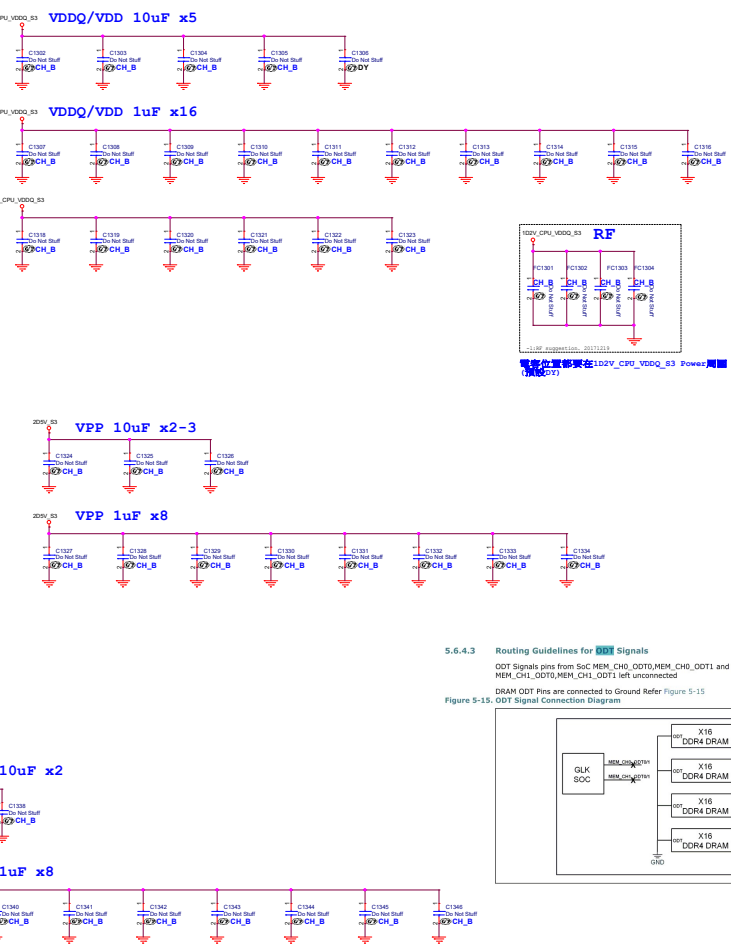
- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87

- 5 M_B_CLK0
- 5 M_B_ACT_N
- 5 M_B_DQ80/81
- 5 M_B_DQ82/83
- 5 M_B_DQ84/85
- 5 M_B_DQ86/87



DDR4 On Board RAM Power Decouple Cap



5.6.4.3 Routing Guidelines for **ODT** Signals
ODT Signals pins from SOC MEM_CH0_ODT0/MEM_CH0_ODT1 and MEM_CH1_ODT0/MEM_CH1_ODT1 left unconnected
DRAM ODT Pins are connected to Ground Refer Figure 5-15
Figure 5-15. ODT Signal Connection Diagram

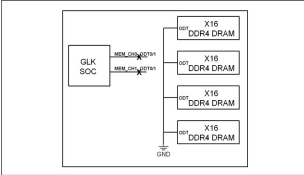


Figure 5-14. Memory Down DRAM_VREF Generation Example Circuit

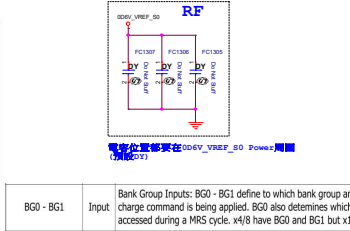
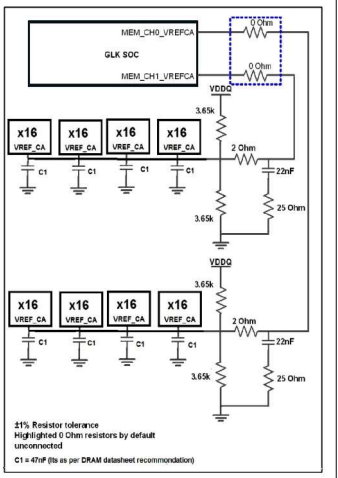


Table 5-14. DDR4 Memory Down (Double-T) Decoupling Recommendation

Memory Configuration	Power Domain	Decoupling Location	Quantity X uF (Size)	Notes
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 Per DRAM as close as possible to the VDD pins of DRAM	32x 1uF (0402)	2
	Vpp	Distribute evenly across domain, close by Drams	10x 10uF (0603)	2
	Vpp	2 as near each x16 DRAM device as possible	16x 1uF (0402)	2
	VTT	Distribute evenly across domain, close by Drams	5x 10uF (0603)	2
DDR4 Memory Down 1x16 (4 device) Each channel	VDD/VDDQ	4 as near each x16 DRAM device as possible	32x 1uF (0402) (All stuffed)	2
	Vpp	Distributed around the DRAM device	10x 10uF (0603) (All stuffed)	2
	Vpp	2 as near each x16 DRAM device as possible	16x 1uF (0402)	2
	VTT	Distributed around the DRAM device	5x 10uF (0603)	2

Notes:
1. The decoupling solution can be taken as an reference, suggest customer to perform completed simulation and validation to verify the solution.
2. Total quantity is referring to 2 channels.
3. Decoupling for the DDR4 Memory Down will also be depend on the DRAM memory requirements itself. Check with DRAM vendor for additional requirements or specifications.

Blanking

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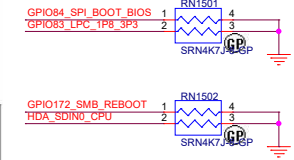
4GB No eMMC

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DDR (Reserved)			
Size A4	Document Number Sapporo_GLK		Rev -1M
Date: Tuesday, February 13, 2018		Sheet 14 of	106

GPIO	GPIO_27	GPIO_28	GPIO_42	GPIO_45	GPIO_61	GPIO_65	GPIO_66
Schematic							
High	Enable =default=	Enable =default=	Override Normal	Enable =debug=	Enable	Force	Boot form LPC
Low	Disable	Disable	No Override	Disable =default=	Disable =default=	Not Force =default=	Not form LPC =default=
GPIO	GPIO_83	GPIO_84	GPIO_163	GPIO_168	GPIO_172	GPIO_174	GPIO_175
Schematic							
High	Buffer set 1.8v	Disable boot from SPI	1.8v	1.8v	Enable	1.24v	eSPI mode
Low	Buffer set 3.3v =default=	Enable boot from SPI =default=	3.3v =default=	3.3v =default=	Disable =default=	1.20v =default=	LPC mode =default=

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDSI_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Note: This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.

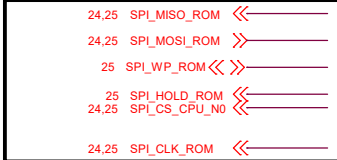
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Notes: 1. DnX: Download and Execute 2. This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB.TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) Note: The board should strap this low and do not use otherwise
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_SDI	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_SDI	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) Note: Platforms should strap this LOW. Functionality is handled by the PMC.



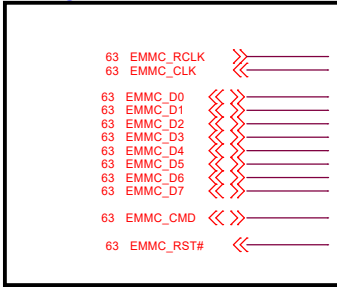
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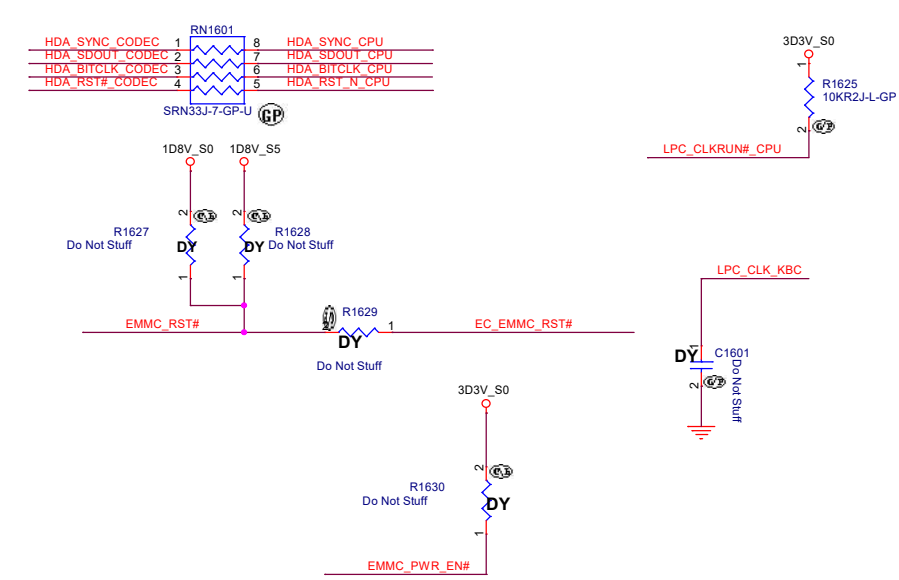
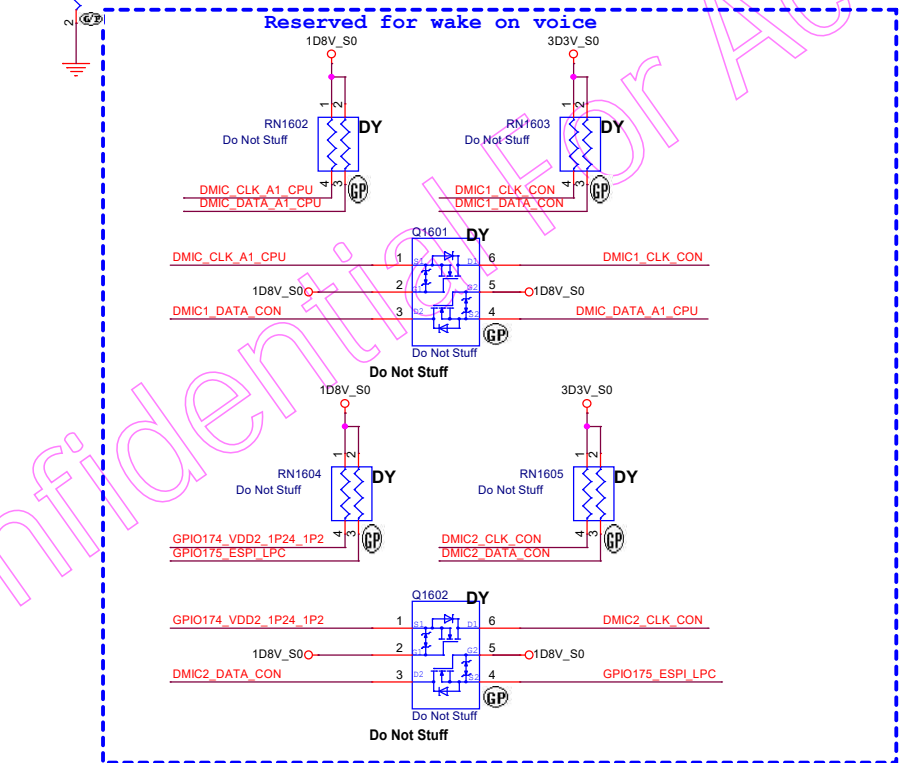
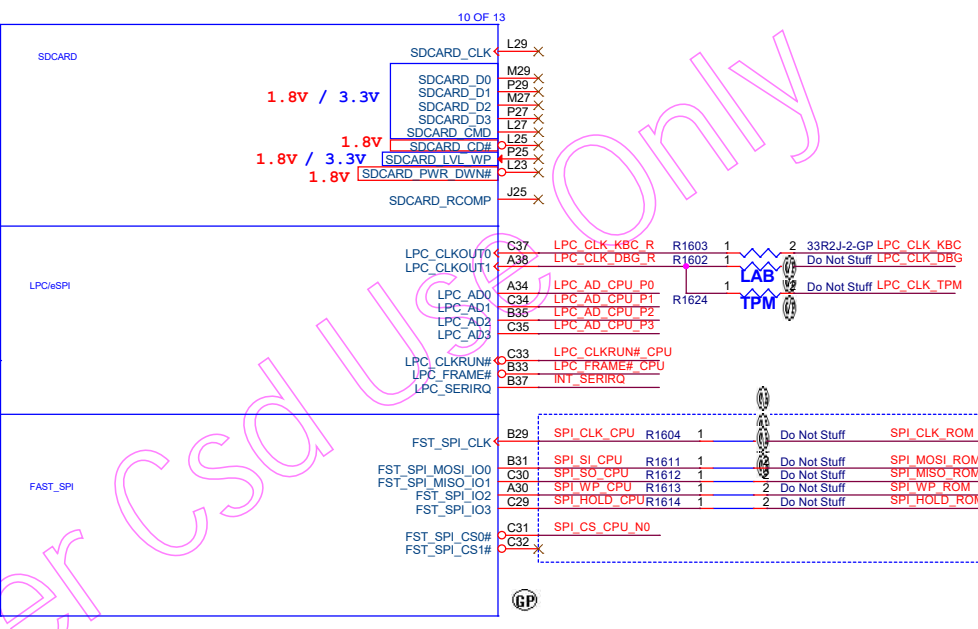
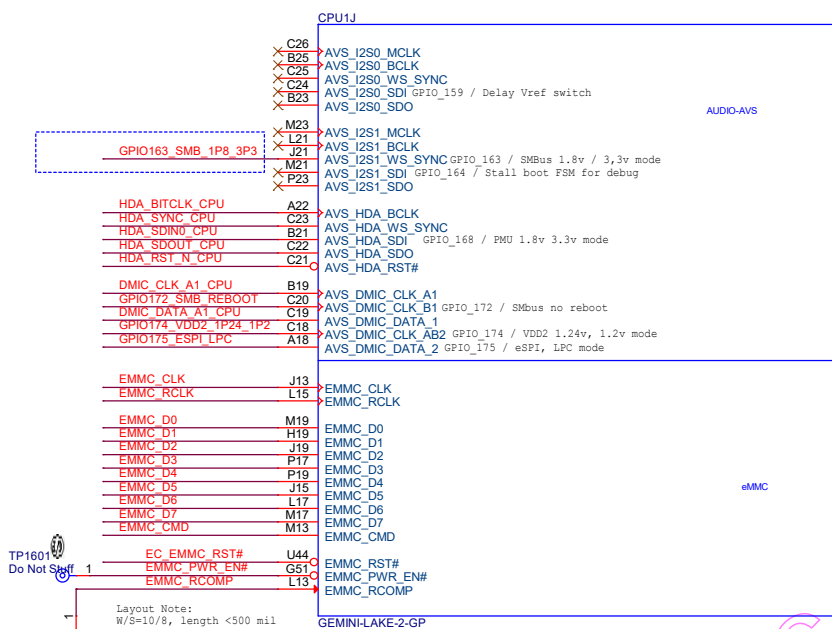
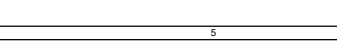
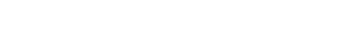
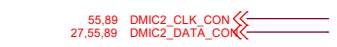
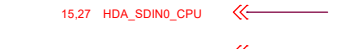
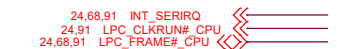
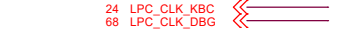
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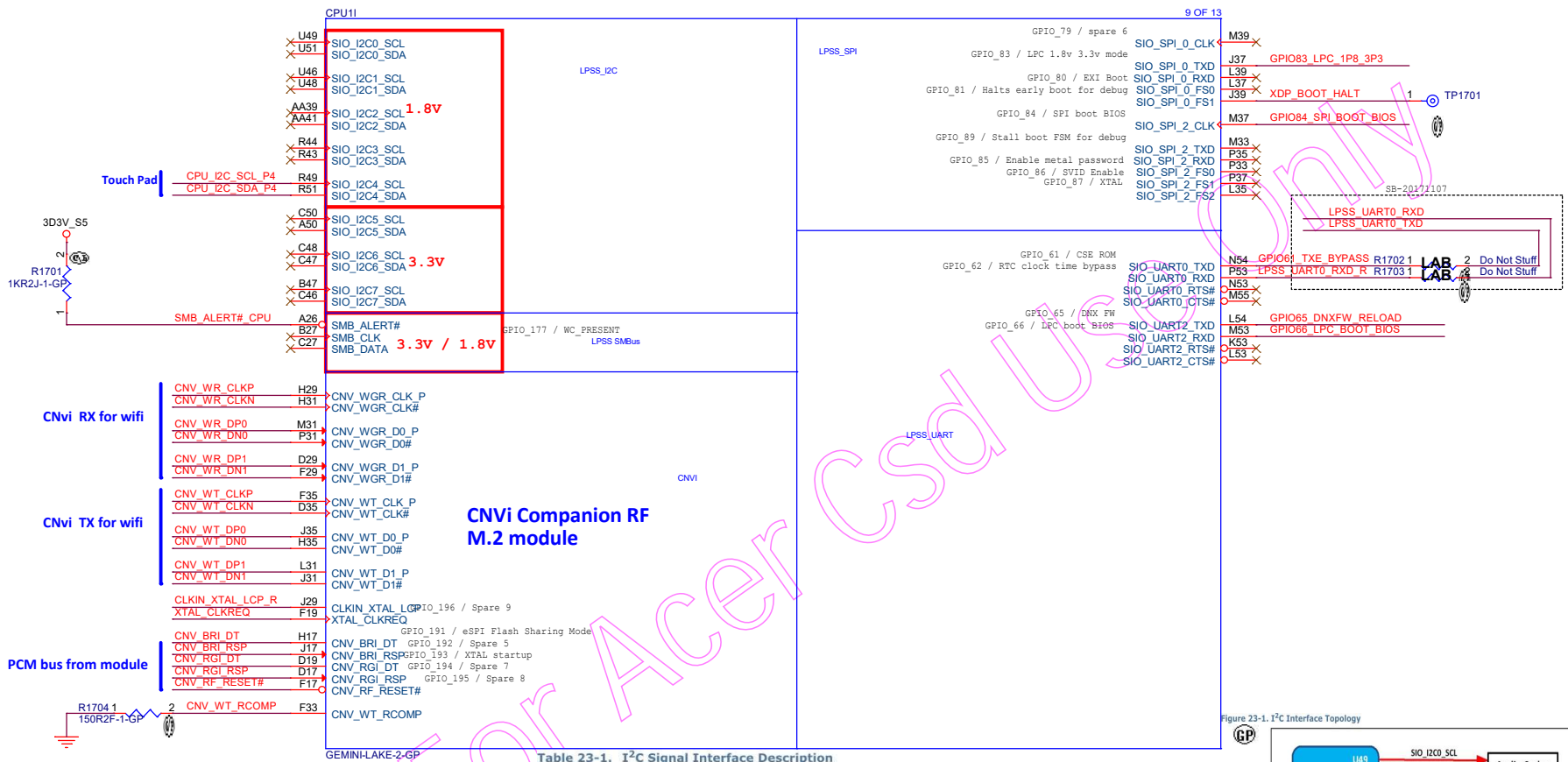
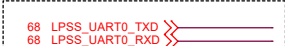
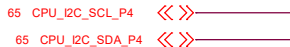
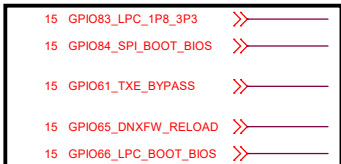
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STRAP



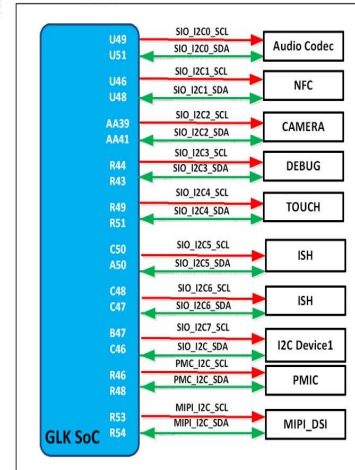
SSID = PCH

Table 23-1. I²C Signal Interface Description

Signal Name	Direction	Maximum Frequency/ Data Rate	Description
SIO_I2C0_SDA SIO_I2C0_SCL	Input/Output Output	3.14MHz	I ² C clock and data for Audio Codec
SIO_I2C1_SDA SIO_I2C1_SCL	Input/Output Output	3.14MHz	I ² C clock and data for NFI or any other I ² C interface
SIO_I2C2_SDA SIO_I2C2_SCL	Input/Output Output	3.14MHz	I ² C clock and data for CAMERA or any other I ² C interfaces
SIO_I2C3_SDA SIO_I2C3_SCL	Input/Output Output	3.14MHz	I ² C clock and data for DEBUG or any other I ² C interfaces
SIO_I2C4_SDA SIO_I2C4_SCL	Input/Output Output	3.14MHz	I ² C clock and data for Touch panel or any other I ² C interfaces
SIO_I2C5_SDA SIO_I2C5_SCL	Input/Output Output	3.14MHz (Note 3)	I ² C clock and data for ISH or any other I ² C interface
SIO_I2C6_SDA SIO_I2C6_SCL	Input/Output Output	3.14MHz (Note 3)	I ² C clock and data for ISH or any other I ² C interface
SIO_I2C7_SDA SIO_I2C7_SCL	Input/Output Output	3.14MHz (Note 3)	I ² C clock and data for any other I ² C interfaces
PMC_I2C_SDA PMC_I2C_SCL	Input/Output Output	3.14MHz	I ² C clock and data for PMI or any other I ² C interface
MIPI_I2C_SDA MIPI_I2C_SCL	Input/Output Output	3.14MHz	I ² C clock and data for DS or any other I ² C interface

Notes:

1. The I²C port assignment refers to the CRB implementation. It is an example of how the I²C ports can be configured.
2. For LPSS I²C ports muxed with ISH I²C ports, refer Gemini Lake SoC – External Design Specification (EDS) and choose the appropriate port function.
3. At 3.3V Mode Port 5, 6 and 7 support up to 1MHz Data rate only. Data rate 1.7MHz and 3.14MHz not supported at 3.3V Mode.



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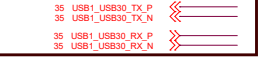
To configure the I²C ports, follow the pin muxing options listed out in the Gemini Lake SoC - External Design Specification (EDS).

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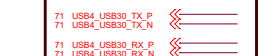
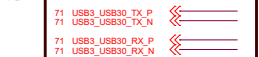
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CPU (I2C/SMB/SPI/UART/CNV1)			
Size	Document Number	Rev	
A3		-1M	
Sapporo GLK			
Date:	Tuesday, February 13, 2018	Sheet	17 of 106

SSID = CPU

USB3.0 Type A



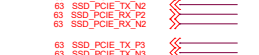
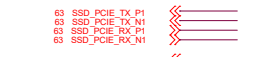
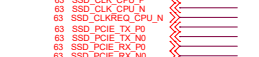
TypeC



WLAN



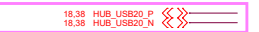
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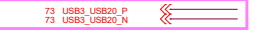
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USB Hub



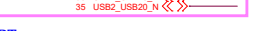
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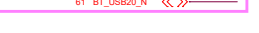
USB3.0 Port1



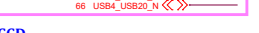
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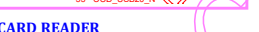
BT



USB 2.0 Type(DB)



CCD



CARD READER



USB Hub

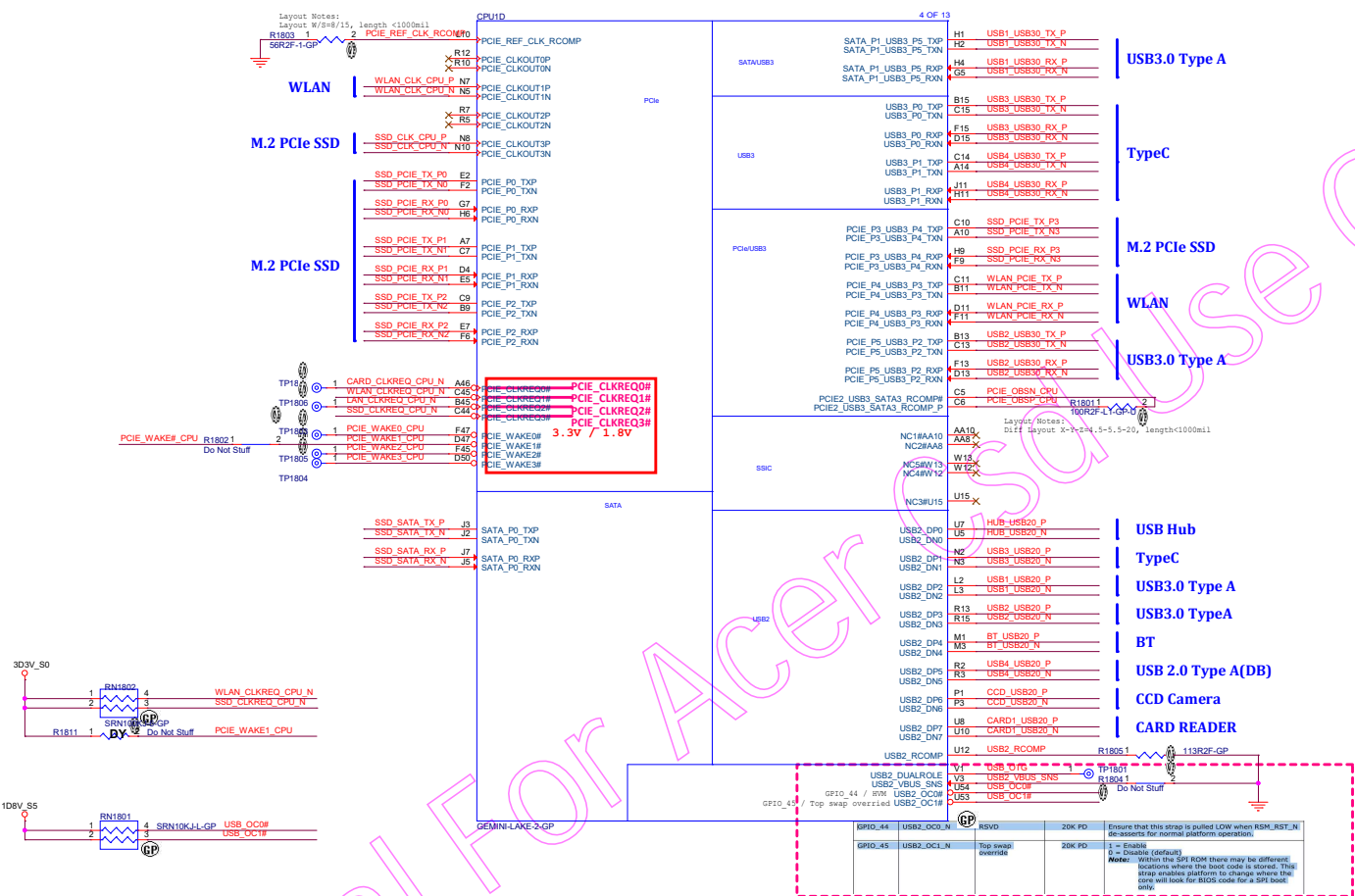
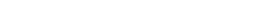
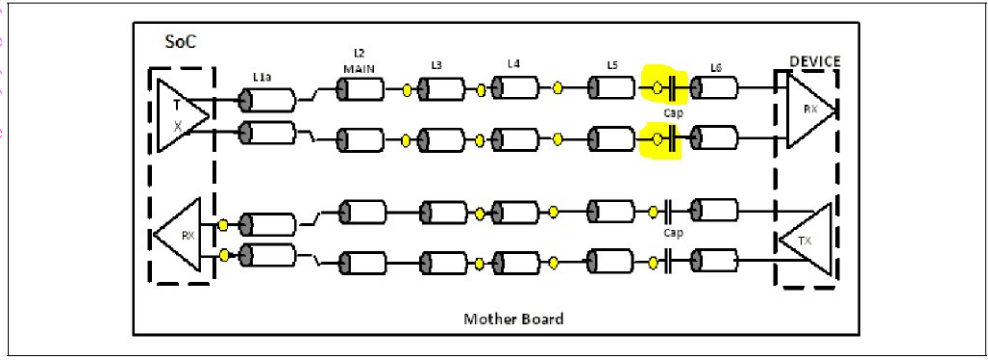
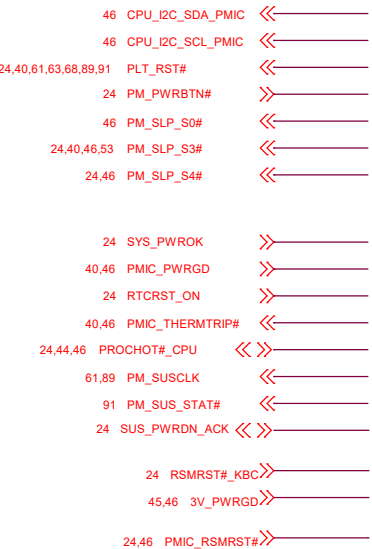
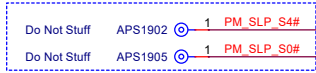


Figure 9-8. PCI Express* Device Down Topology

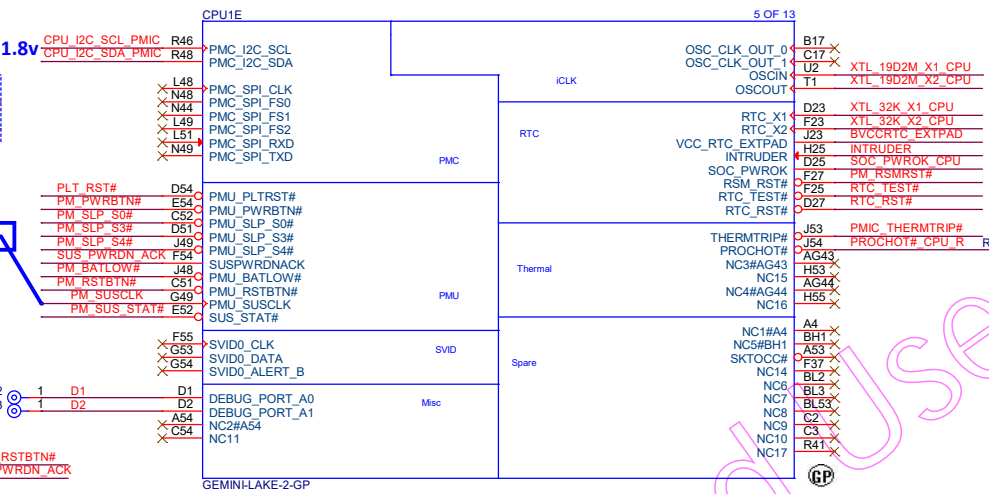
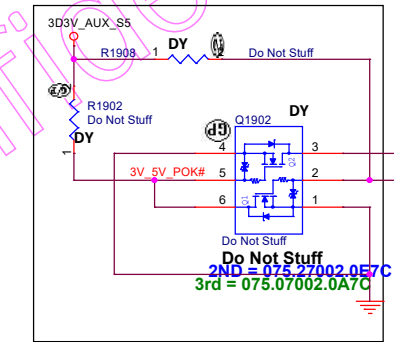
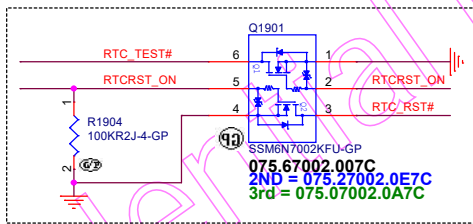
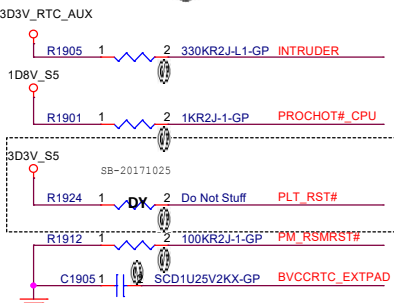
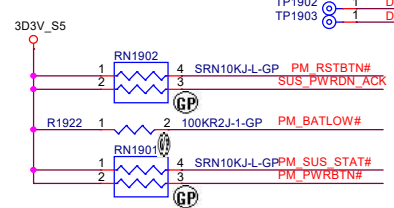




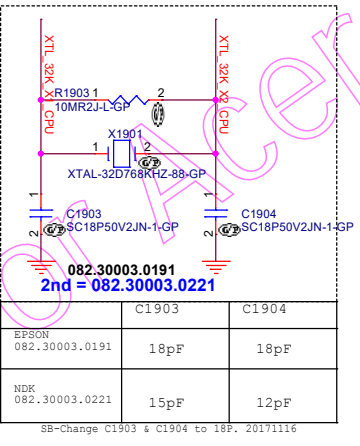
APS debug port



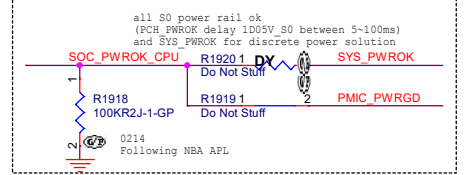
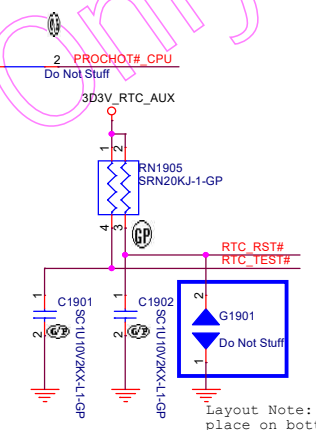
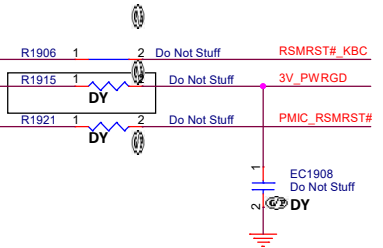
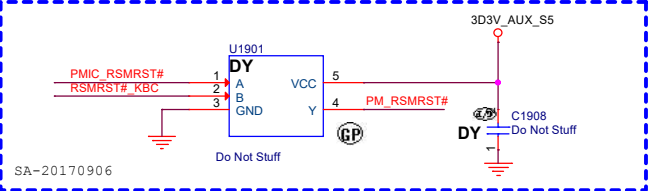
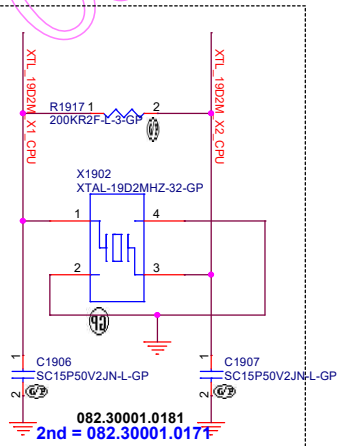
32kHz for CNVi pin50



32.768 kHz



19.2 MHz



19.2MHz 8PFC
TYPW = 35 ppm
CLOAD (MAX) 11pF

	C1901	C1902
0820001 082.30001.0181	15pF	15pF
082 082.30001.0177	15pF	15pF
082 082.30001.0155	15pF	15pF

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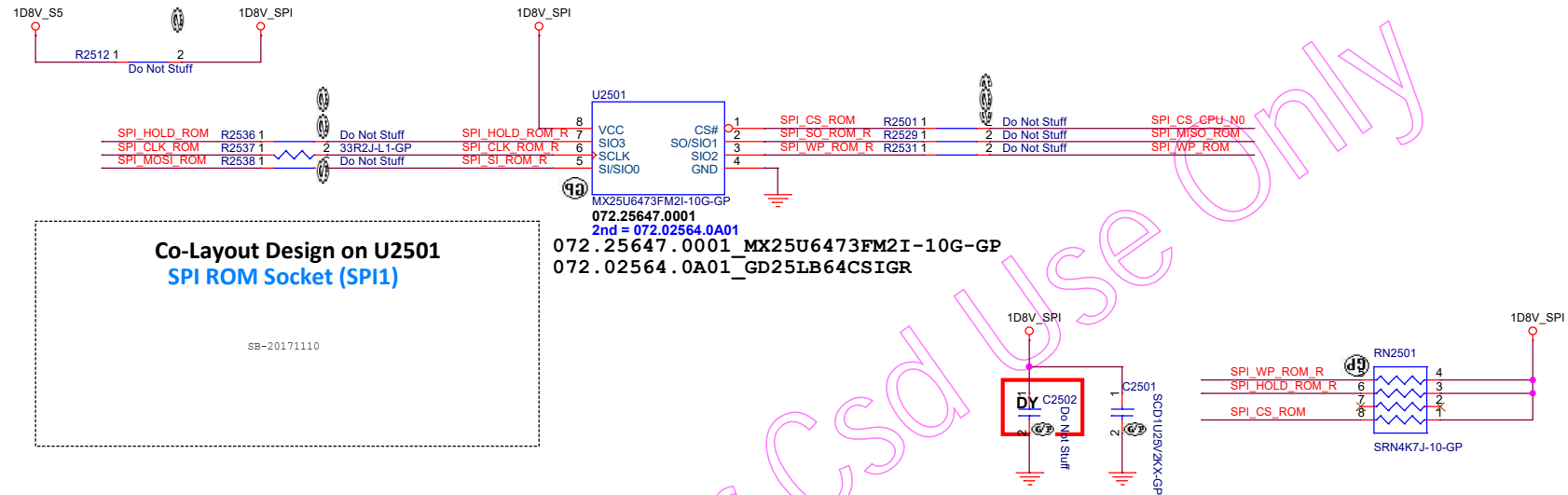
-1M

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

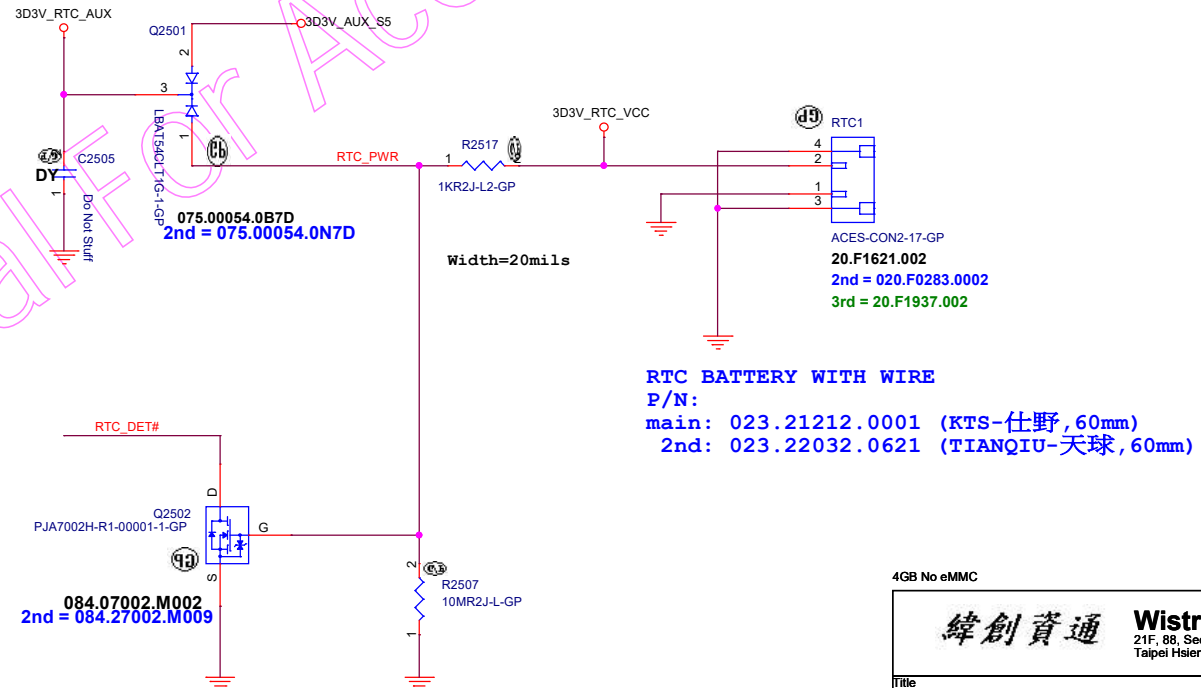
16 SPI_HOLD_ROM <<<
16,24 SPI_CLK_ROM <<<
16,24 SPI_MOSI_ROM <<<

16,24 SPI_CS_CPU_N0 <<<
16,24 SPI_MISO_ROM <<<
16 SPI_WP_ROM <<<



SSID = RBAT

20 RTC_DET# <<<



RTC BATTERY WITH WIRE

P/N:

main: 023.21212.0001 (KTS-仕野, 60mm)

2nd: 023.22032.0621 (TIANQIU-天球, 60mm)

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Title

Flash/RTC

Size
Custom

Document Number

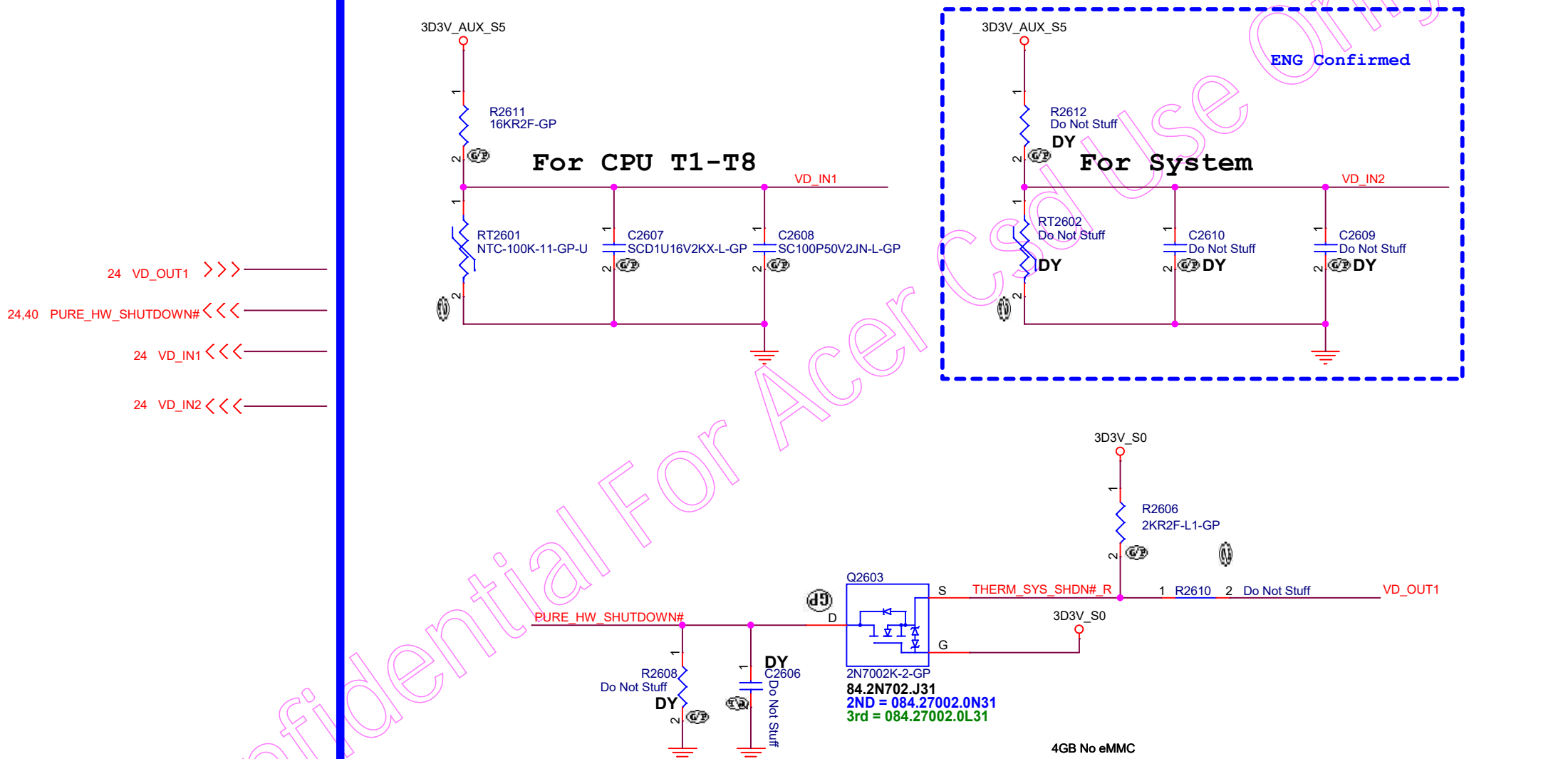
Sapporo_GLK

Rev
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Main Func = Thermal Sensor



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INT IO(THERMAL)					
Size	Document Number				Rev
A4	Sapporo GLK				-1M
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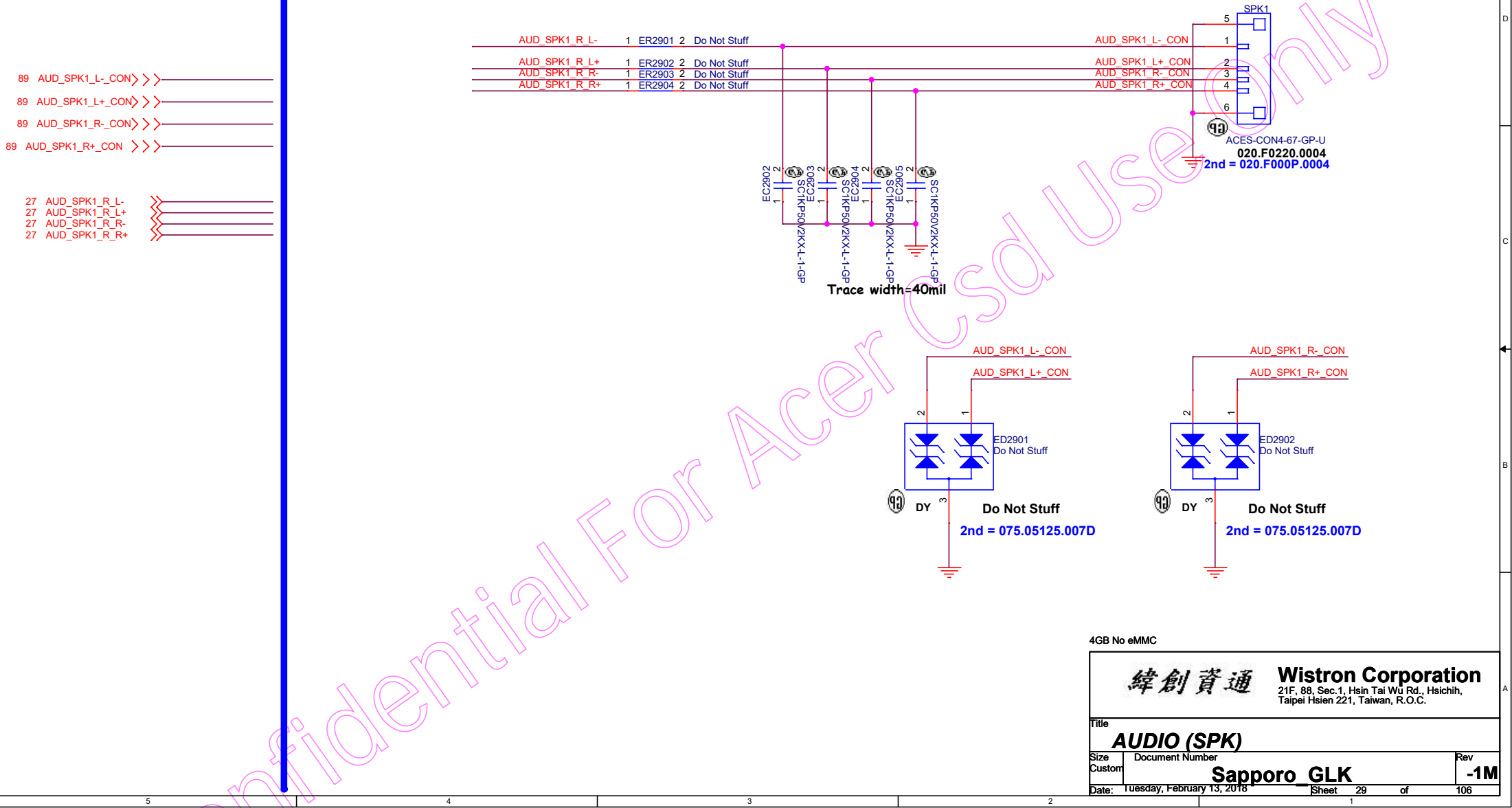
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Title (Reserved) Audio AMP			
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SSID = AUDIO *Speaker*



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Title AUDIO (SPK)			
Size	Document Number	Rev	
Custom	Sapporo GLK	-1M	
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Title

Reserved (USB2.0 CONN)

Size
A4

Document Number

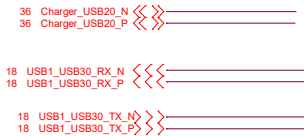
Sapporo_GLK

Rev
-1M

Date: Tuesday, February 13, 2018

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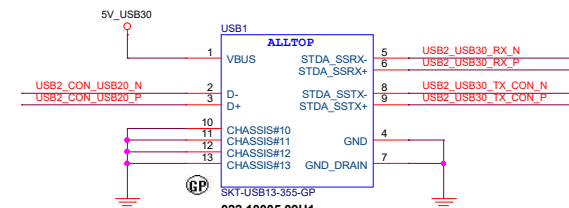
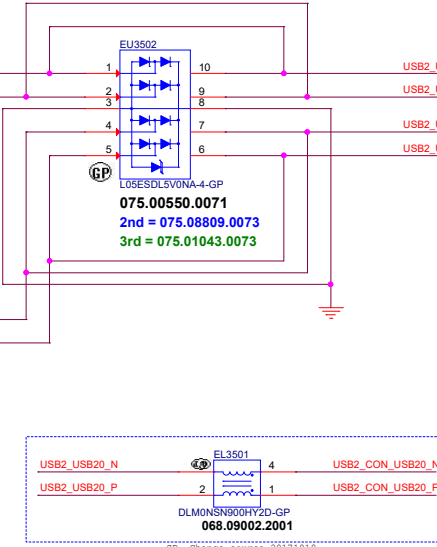
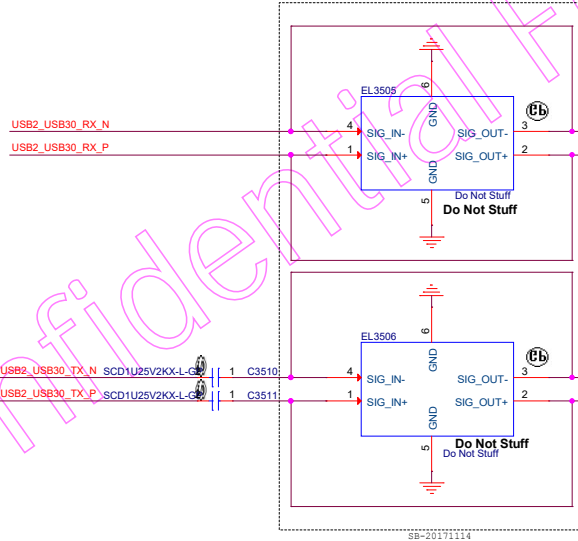
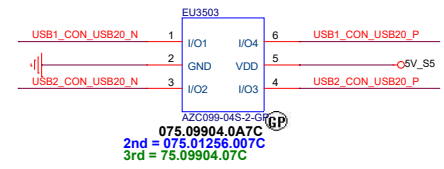
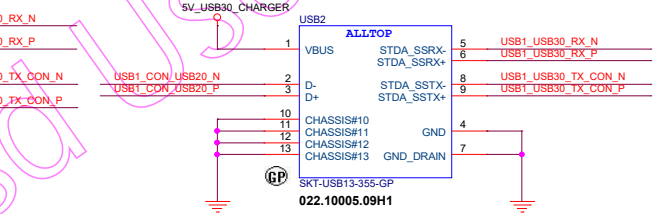
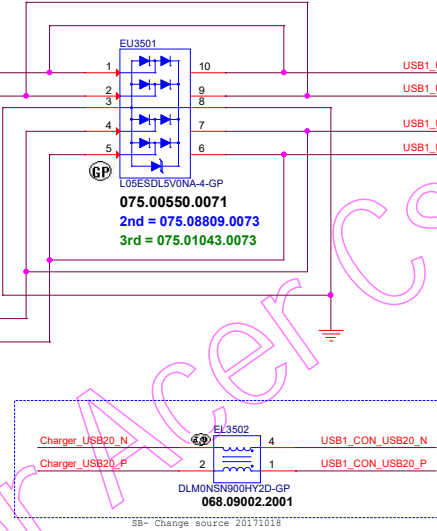
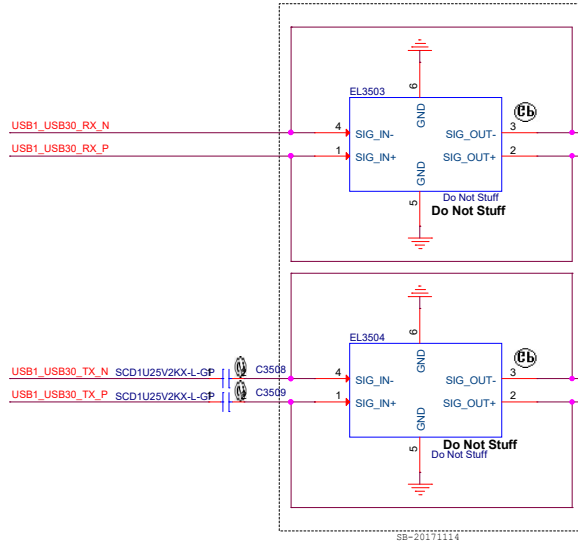
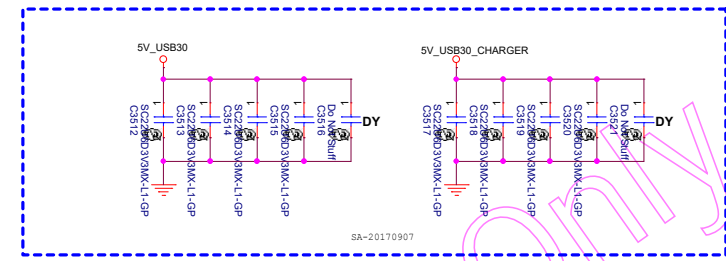
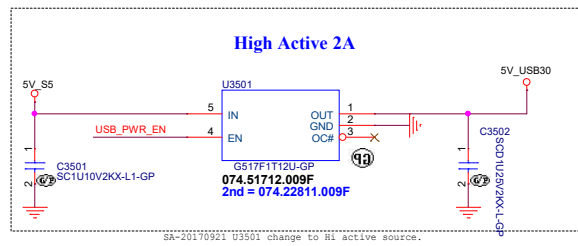
USB1



USB2



USB Power enable



5.PIN DEFINE TABLE:

PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	GND

PIN NO.	5	6	7	8	9
SIGNAL NAME	StdA_SSRX-	StdA_SSRX+	GND-DRAIN	StdA_SSTX-	StdA_SSTX+

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Title **USB (USB3.0 Conn)**

Size Custom Document Number **Sapporo GLK** Rev **-1M**

Date: Tuesday, February 13, 2018 1 Sheet 35 of 106

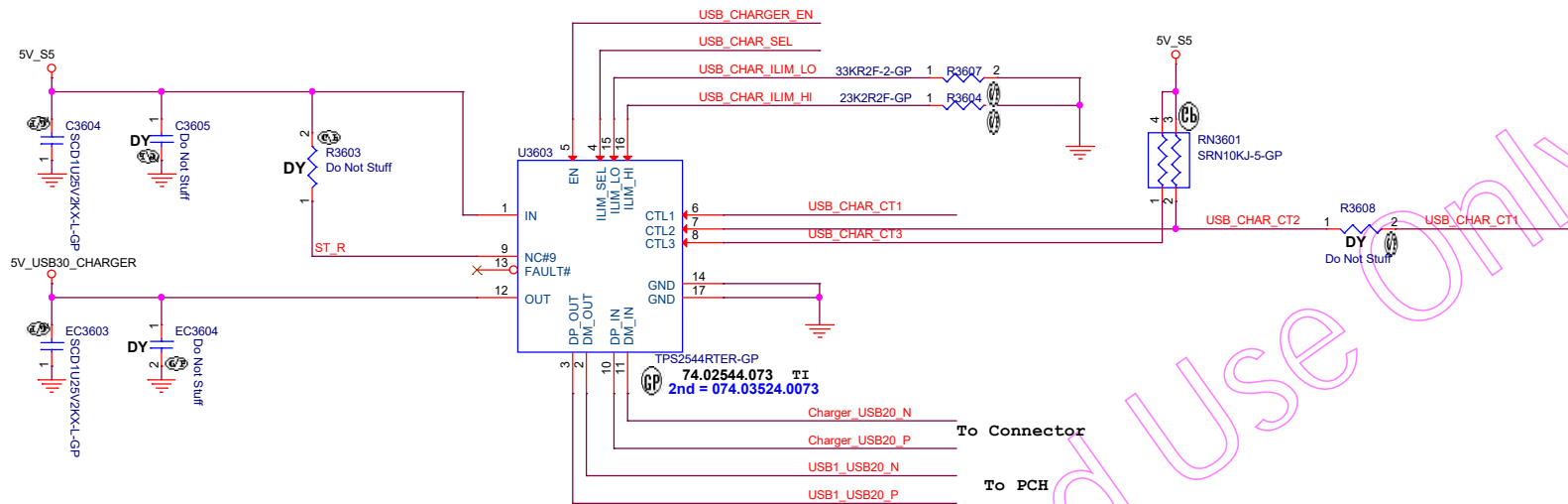
24 USB_CHARGER_EN >>>
 24 USB_CHAR_SEL >>>
 24 USB_CHAR_CT1 >>>

To Connector

35 Charger_USB20_N <<<
 35 Charger_USB20_P <<<

To PCH

18 USB1_USB20_N <<<
 18 USB1_USB20_P <<<



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2	ILIM_LO	Data Lines Connected
1	1	1	1	CDP ⁽¹⁾	ILIM_HI	

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Title: **USB(USB Charger)**
 Size: Custom Document Number: **Sapporo GLK** Rev: **-1M**
 Date: Tuesday, February 13, 2018 Sheet 36 of 106

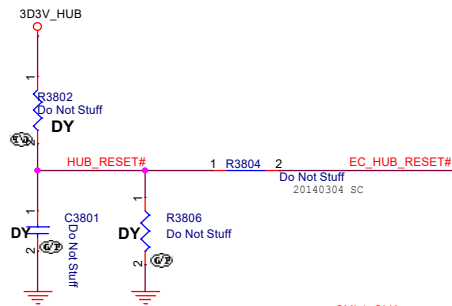
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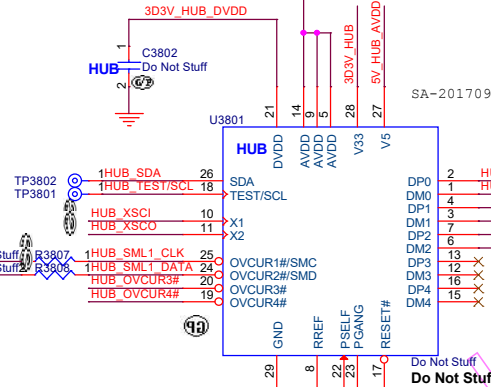
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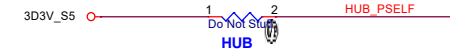
18 HUB_USB20_P
18 HUB_USB20_N
55 TS_USB20_P
55 TS_USB20_N
66 FP_USB20_P
66 FP_USB20_N
24 SML1_CLK
24 SML1_DATA
24 EC_HUB_RESET#



SML1_CLK HUB_SMB_MODE
SML1_DATA HUB_SMB_MODE

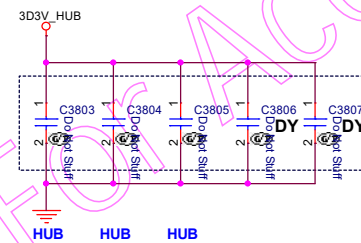
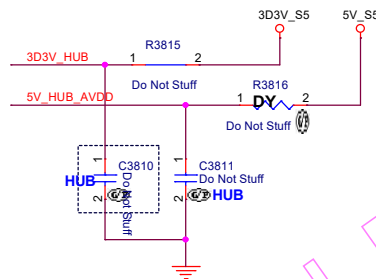


SA-20170907-Change Symbol

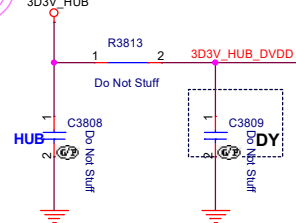


FP_USB20_P
FP_USB20_N

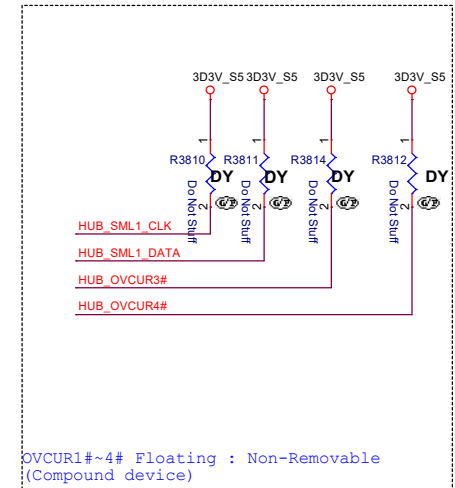
CPU
TUCH PABEL
Finger print



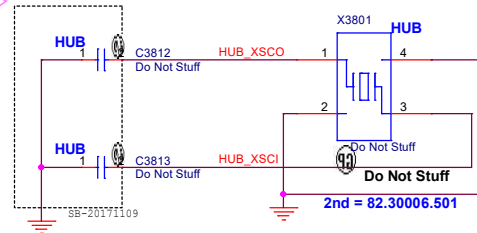
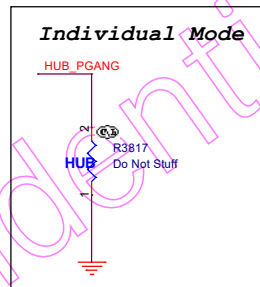
As close to GL850G-32



EC1 close to
PIN28



OVCUR1#~4# Floating : Non-Removable
(Compound device)



2nd = 82.30006.501

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USB(HUB)			
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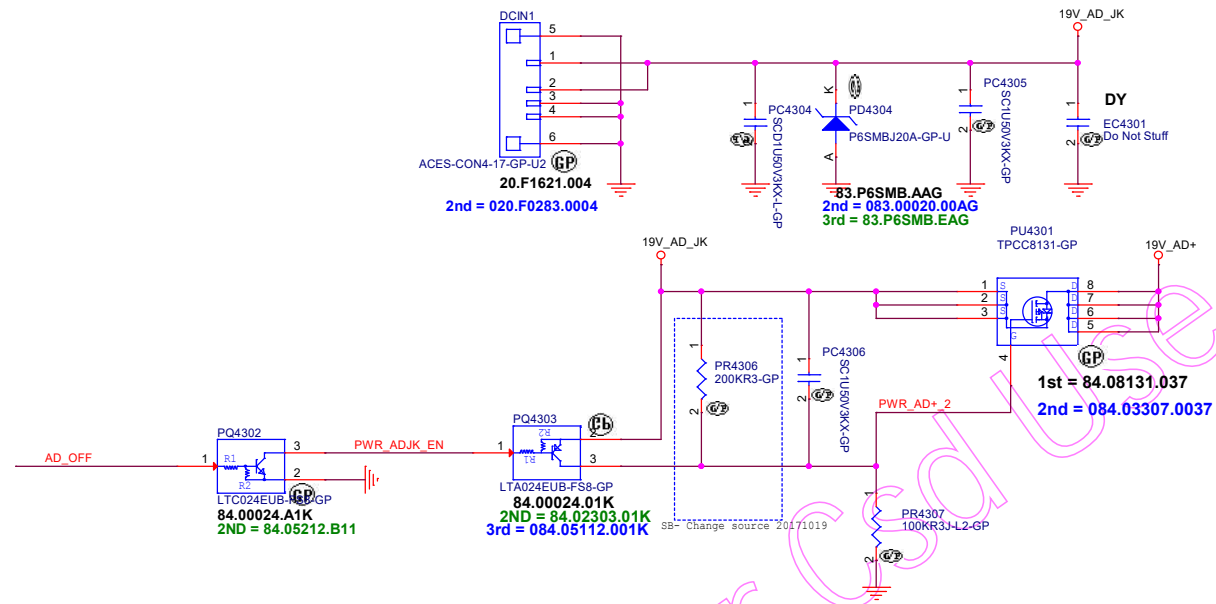
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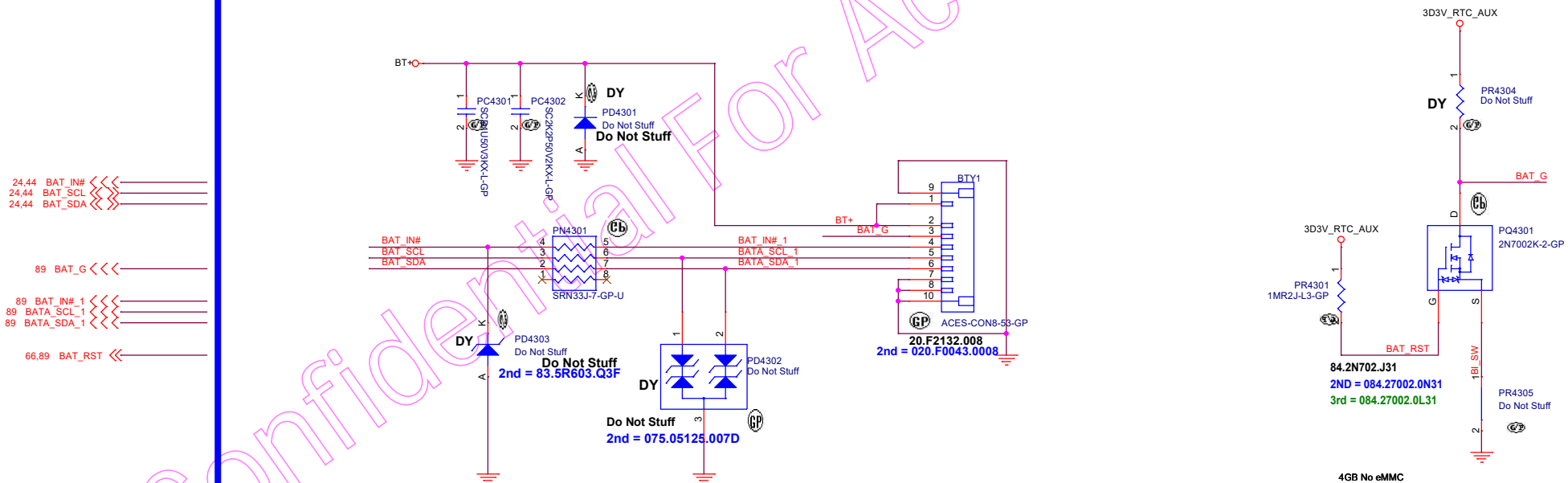
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Title (Reserved)			
Size A4	Document Number Sapporo_GLK		Rev -1M
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ANNIE solution

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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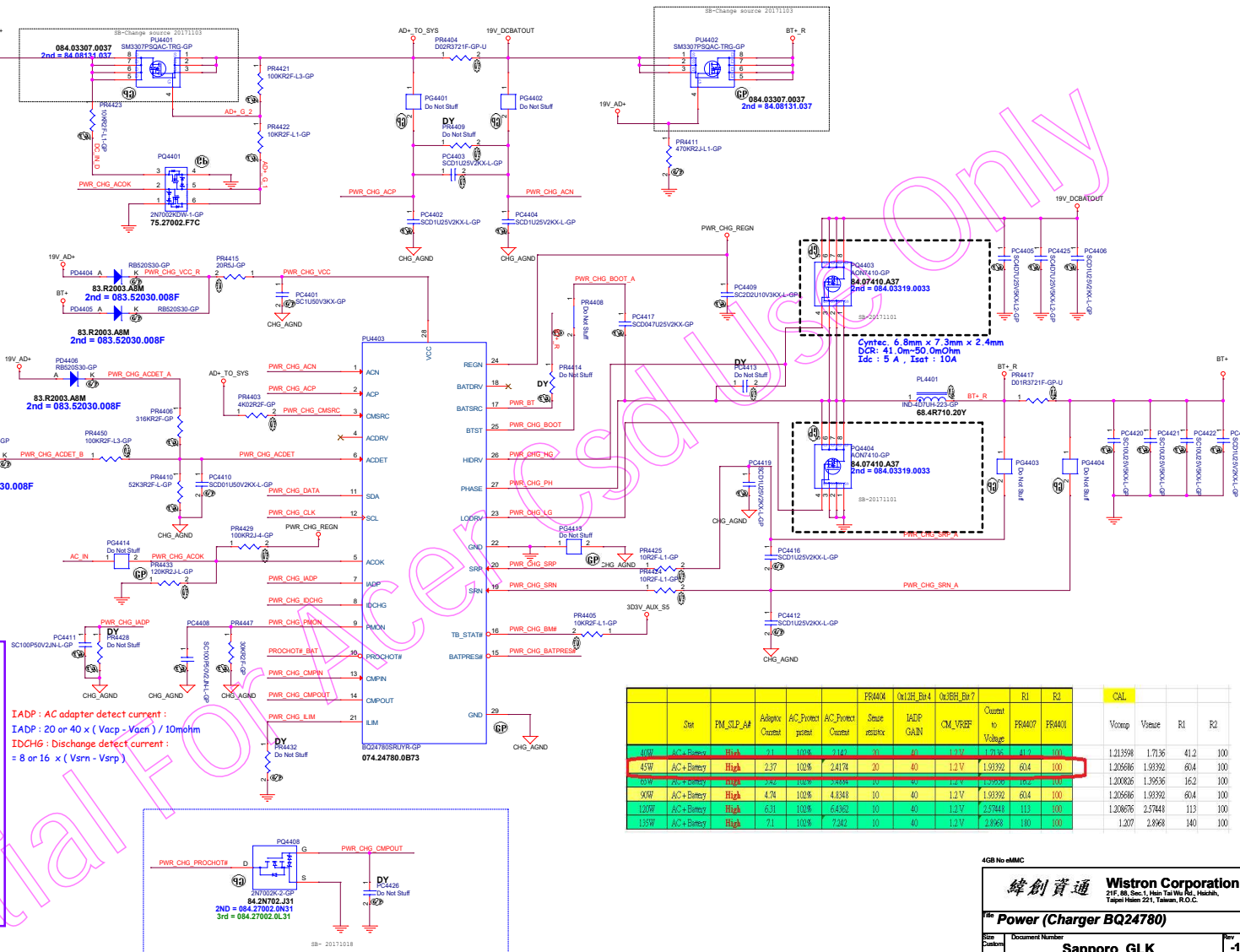
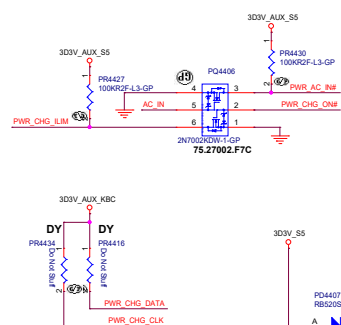
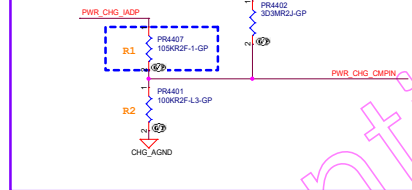
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Title		
INT IO(DC IN/BATT CONN)		
Size	Document Number	Rev
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Sheet 43 of 106		



```
PR4407 45W 73.2K ADT PROTECT 110
PR4407 45W 105K ADT PROTECT 130
PR4407 65W 150K ADT PROTECT 110
PR4407 65W 196K ADT PROTECT 130
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[illegible]

4GB No eMMC

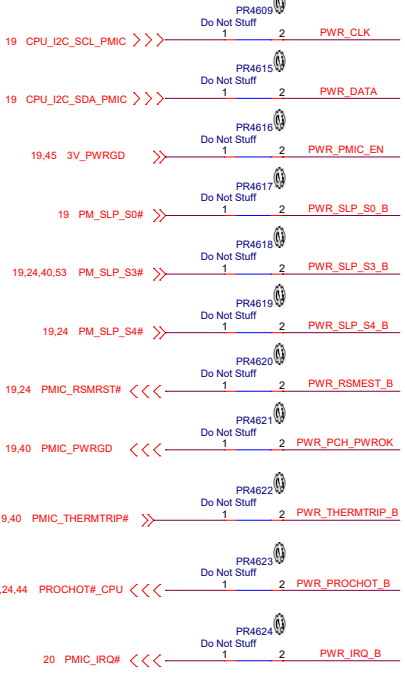
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File **Power (Charger BQ24780)**

Size Custom	Document Number Sapporo GLK	Rev -1
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OFFPAGE



Main Func = CPU_CORE

I2C, Other signals

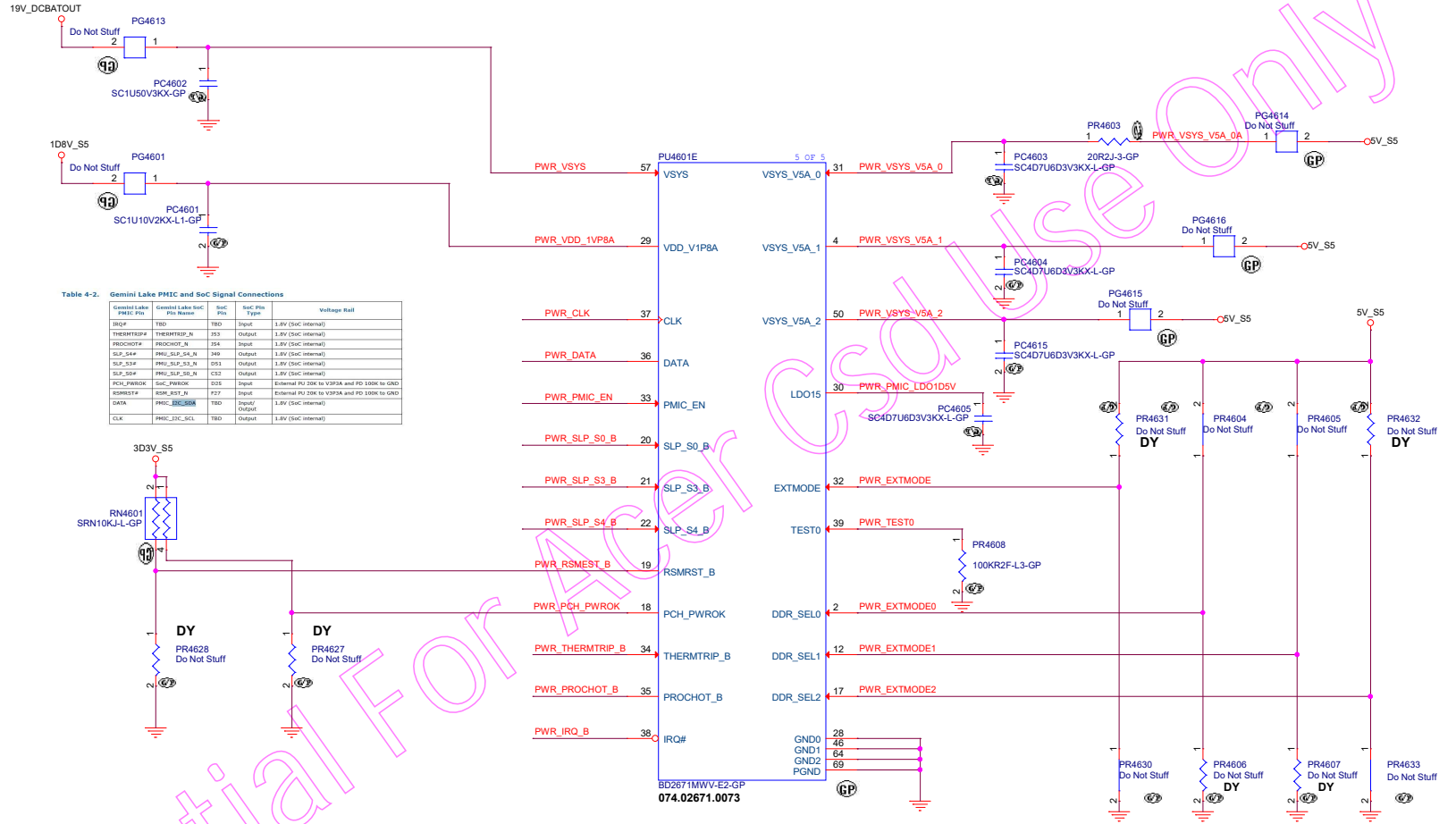


Table 4-2: Gemini Lake PMIC and SoC Signal Connections

Gemini Lake PMIC Pin	Gemini Lake SoC Pin Name	SoC Pin Type	Voltage Rail
TRD0	TRD	Input	1.8V (SoC internal)
THERMTRIP#	THERMTRIP_N	Input	1.8V (SoC internal)
PROCHOT#	PROCHOT_N	Input	1.8V (SoC internal)
SLP_S0#	PMU_SLP_S0_N	Output	1.8V (SoC internal)
SLP_S3#	PMU_SLP_S3_N	Output	1.8V (SoC internal)
SLP_S4#	PMU_SLP_S4_N	Output	1.8V (SoC internal)
RSMRST#	RSMRST_N	Output	1.8V (SoC internal)
PMIC_PWRGD	PMIC_PWRGD	Input	External PU 20K to VDDP8A and PD 100K to GND
PMIC_IRQ#	PMIC_IRQ#	Input	External PU 20K to VDDP8A and PD 100K to GND
CLK	PMIC_CLK	Output	1.8V (SoC internal)

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL0,1	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.20V	1.80V	1.20V	0.60V	-
(L,L,H)	DDR3L	1.35V	OFF	1.20V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.10V	1.80V	1.20V	0.55V	-
(L,H,H)	DDR4	1.20V	2.50V	1.20V	0.60V	-
(H,L,L)	LPDDR3	1.20V (V1P2A boot timing)	1.80V	OFF	0.60V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.35V	1.80V (SLP_S3_B output)	1.20V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.10V	1.80V	1.20V	OFF	VTT unused
(H,H,H)	DDR4	1.20V (V1P2A boot timing)	2.50V	OFF	0.60V	V1P2A merged to VDDQ

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Title: 046_Power(BD2671_I2C)

Size: Custom Document Number: Sapporo_GLK Rev: -1M

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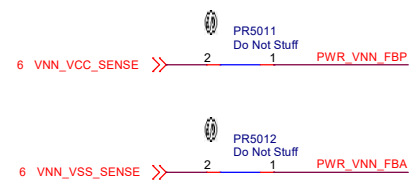
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

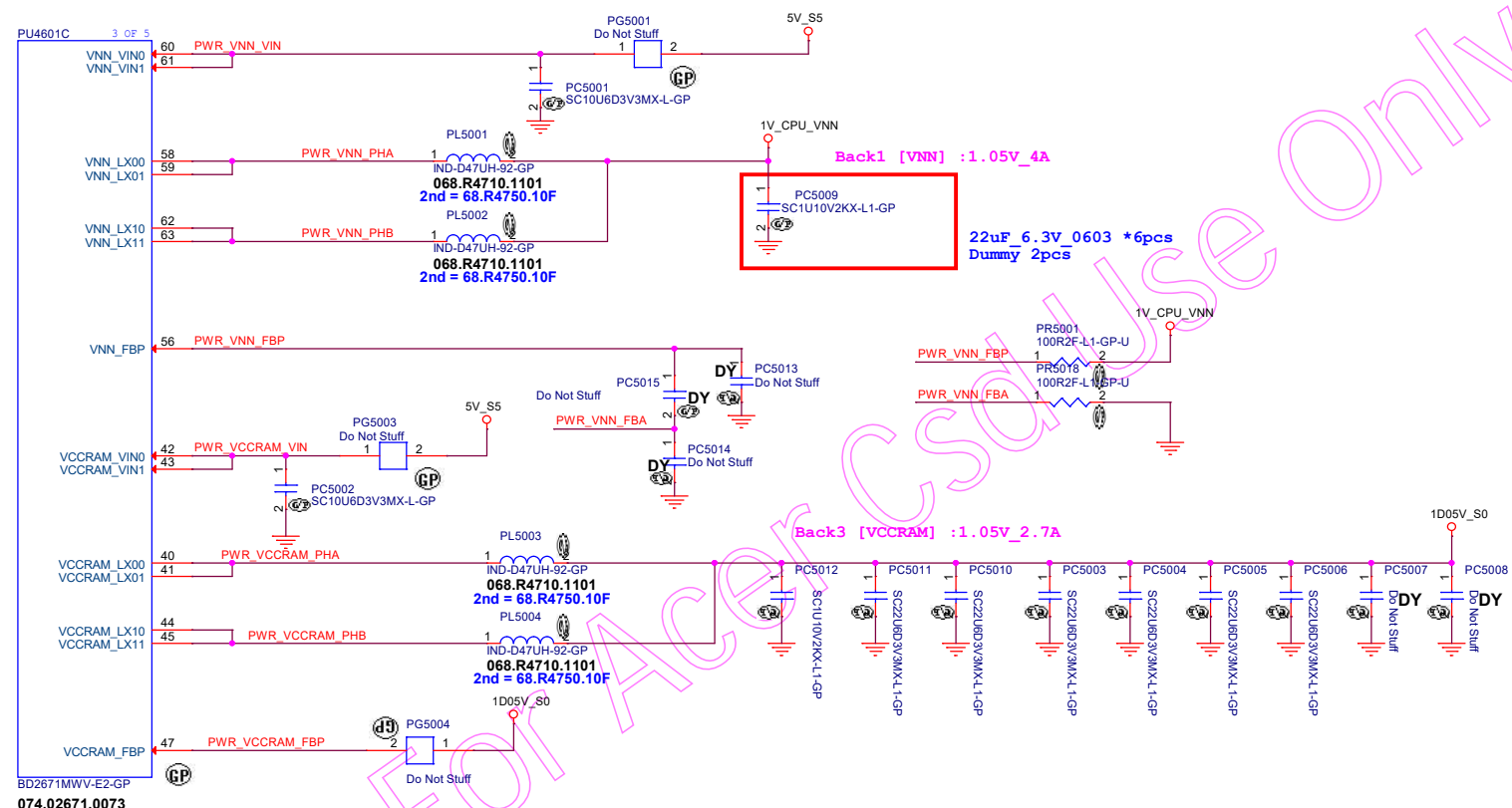
Title
Reserved

Size A4	Document Number Sapporo_GLK	Rev -1M
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Date: Tuesday, February 13, 2018 Sheet 49 of 106



VNN[BUCK1], VCCRAM[BUCK3]



5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence (DDR_SEL2,1,0="000""010""011")

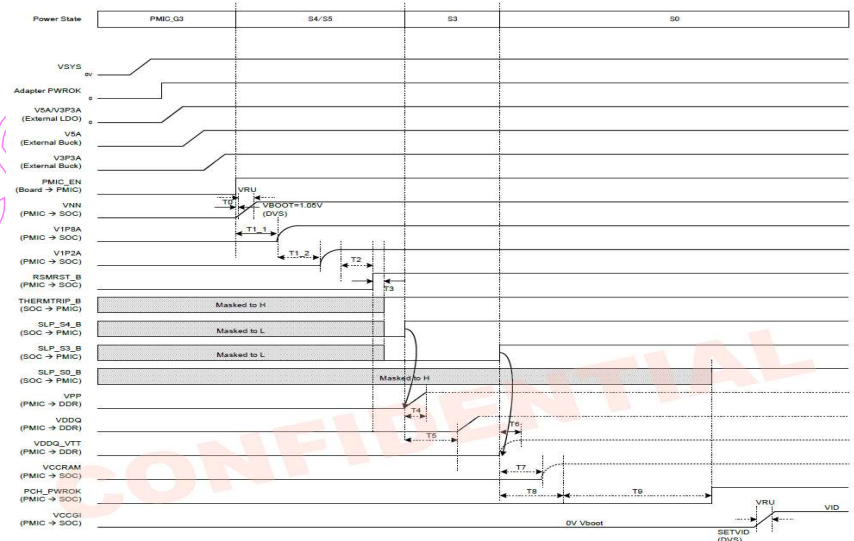


Figure 5-2 G3 to S5/S4 & S5/S4 to S0 Power Sequence

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VDDQ[BUCK6], V1P2A[BUCK5]

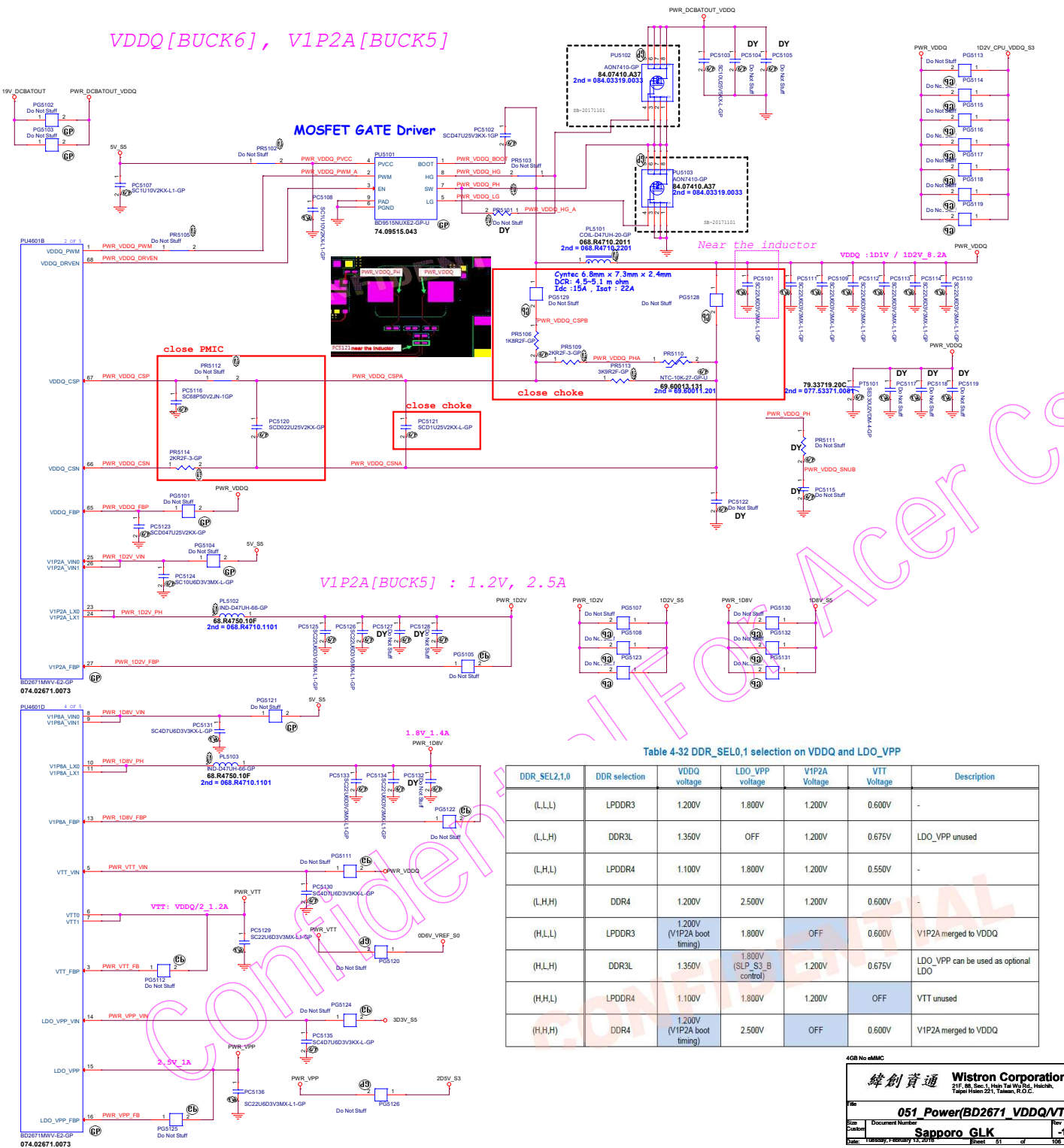


Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

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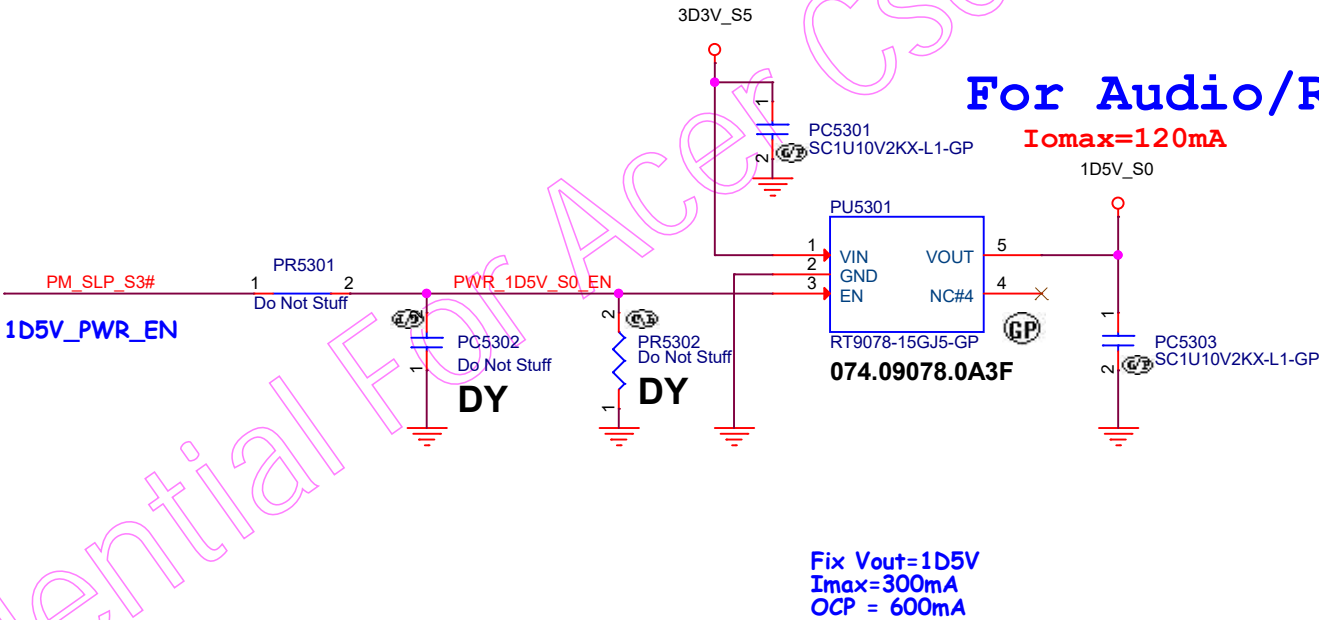
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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RT9078 for 1D5V_S0
Enable=0.9V
Disable=0.4V


For HDMI re-driver and audio codec

For Audio/Re-driver

19,24,40,46 PM_SLP_S3# >>



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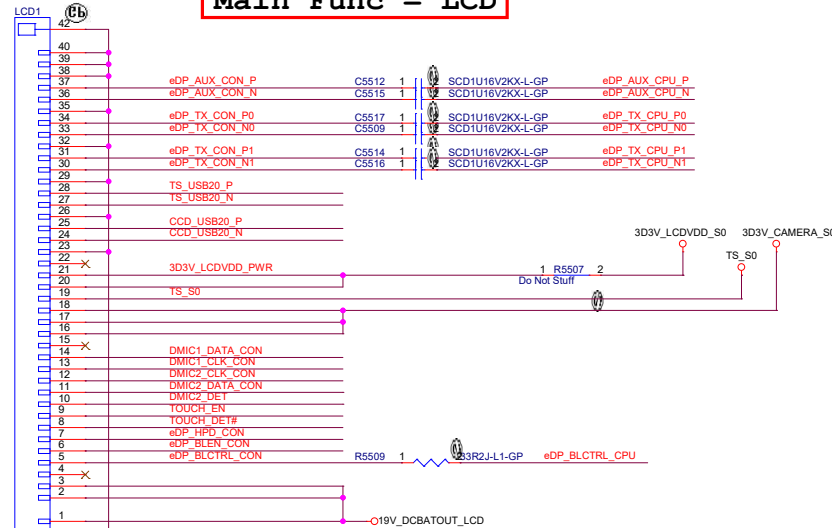
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Title (Reserved)1D8V			
Size A4	Document Number Sapporo_GLK		Rev -1M
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SSID = VIDEO

Panel Conn.

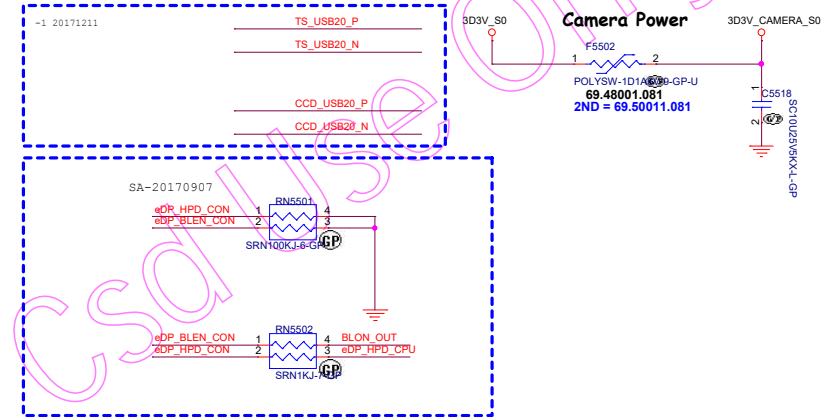
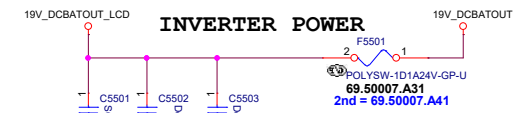
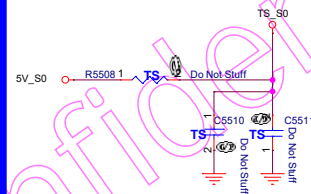
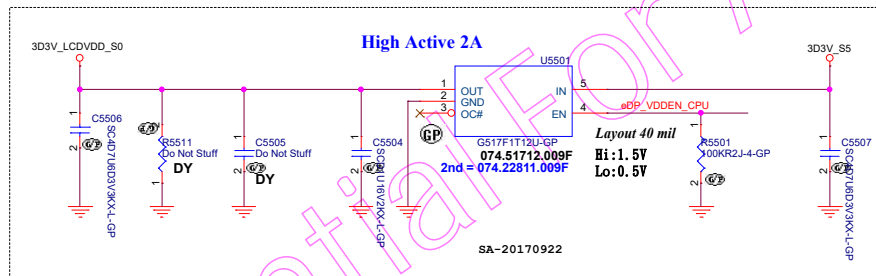
Main Func = LCD

8 eDP_VDDEN_CPU >>>
8 eDP_AUX_CPU_P >>>
8 eDP_AUX_CPU_N >>>
8 eDP_TX_CPU_P0 >>>
8 eDP_TX_CPU_N0 >>>
8 eDP_TX_CPU_P1 >>>
8 eDP_TX_CPU_N1 >>>
24 TOUCH_EN >>>
38 TS_USB20_P <<<
38 TS_USB20_N <<<
18 CCD_USB20_P <<<
18 CCD_USB20_N <<<
24 TOUCH_DET# <<<
27 DMIC_CLK_CON <<<
8 eDP_HPD_CPU <<<
8 eDP_BLCtrl_CPU >>>
24 BLON_OUT >>>
20,89 DMIC2_DET >>>
16,27,89 DMIC2_DATA_CON <<<
16,27,89 DMIC1_DATA_CON <<<
16,89 DMIC1_CLK_CON >>>
16,89 DMIC2_CLK_CON >>>
89 eDP_BLCtrl_CON <<<
89 eDP_BLEN_CON <<<
89 eDP_HPD_CON <<<
89 3D3V_LCDVDD_PWR <<<

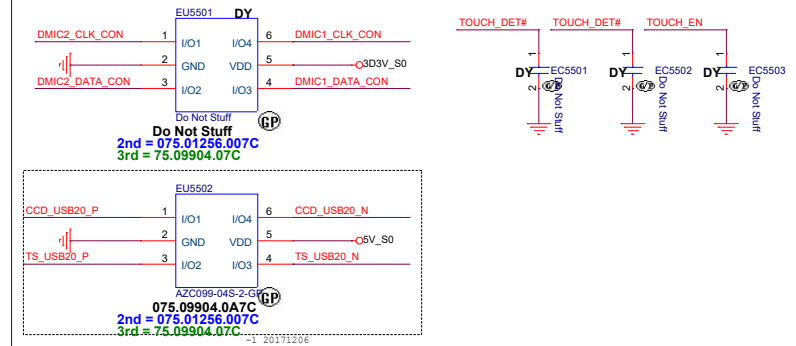


ACES-CON40-18-GP
20.K0678.040
2nd = 20.K0809.040
3rd = 020.K0160.0040

For CCD module--> DMIC1_CLK_CON R5523 1 Do Not Stuff
For DMIC module--> DMIC2_CLK_CON R5522 1 2 Do Not Stuff DMIC_CLK_CON



EMI Request:



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LCD Connector

Size

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Document Number

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Rev
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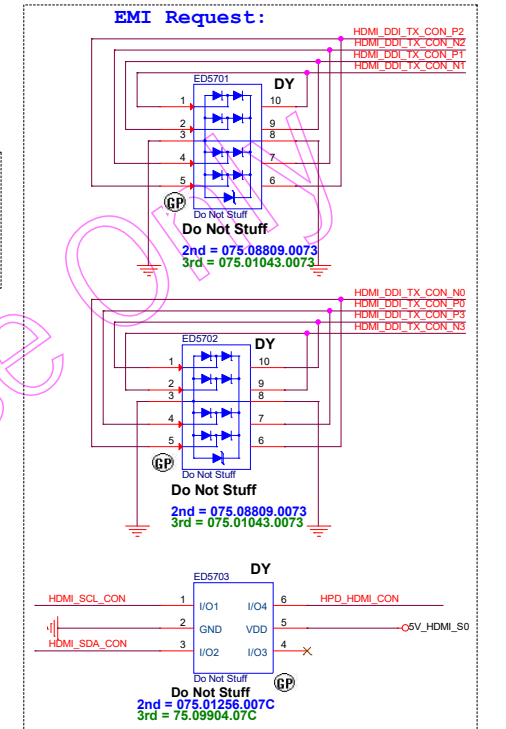
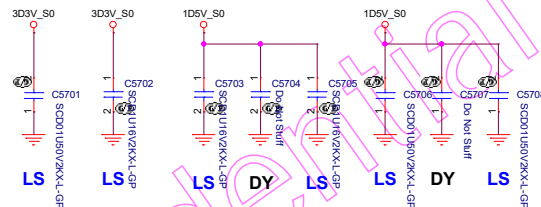
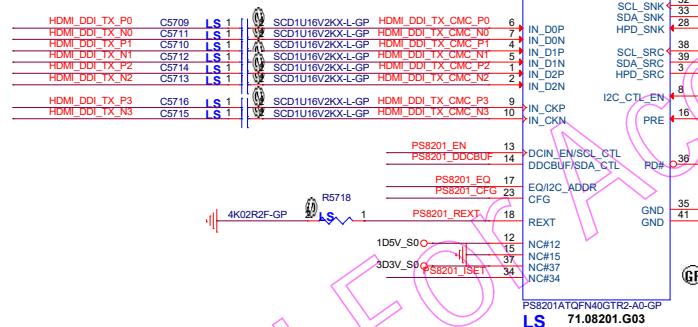
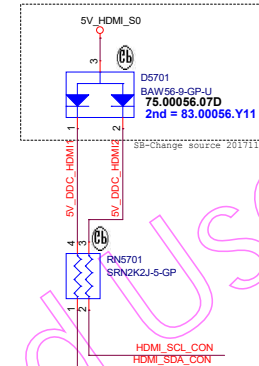
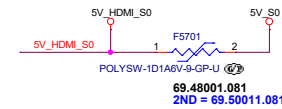
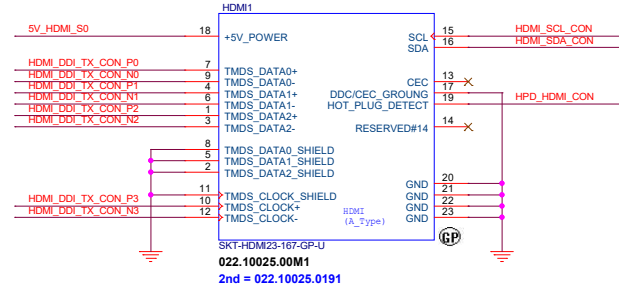
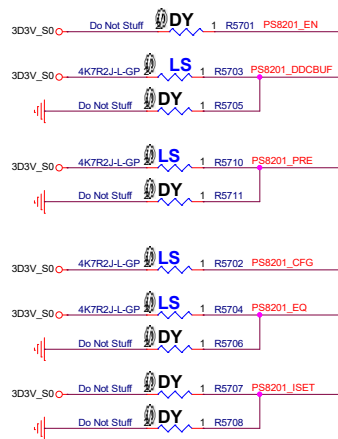
Date: Tuesday, February 13, 2018

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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN



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Wistron Corporation
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Title			Rev
HDMI Level Shifter/Connector			
Size	Document Number	Sapporo GLK	
Custom			
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Title		
(Reserved)HDD/ODD		
Size	Document Number	Rev
A3	Sapporo_GLK	-1M
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SSID = WLAN

CNVI

17	CNV_RF_RESET#	>>	
17	CNV_WR_DN1	<<	
17	CNV_WR_DP1	<<	
17	CNV_WR_DN0	<<	
17	CNV_WR_DP0	<<	
17	CNV_WR_CLKP	<<	
17	CNV_WR_CLKN	<<	
17	CNV_WT_DN1	<<	
17	CNV_WT_DP1	<<	
17	CNV_WT_DN0	<<	
17	CNV_WT_DP0	<<	
17	CNV_WT_CLKN	<<	
17	CNV_WT_CLKP	<<	
17,89	XTAL_CLKREQ	>>	
17	CNV_BRI_RSP	<<	
17	CNV_RGI_DT	<<	
17	CNV_RGI_RSP	<<	
17	CNV_BRI_DT	<<	

BT

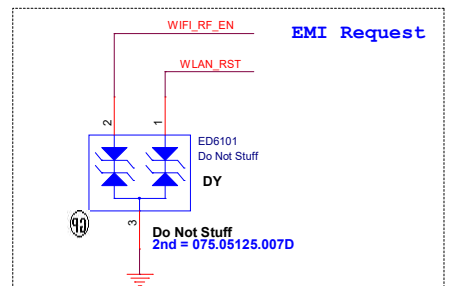
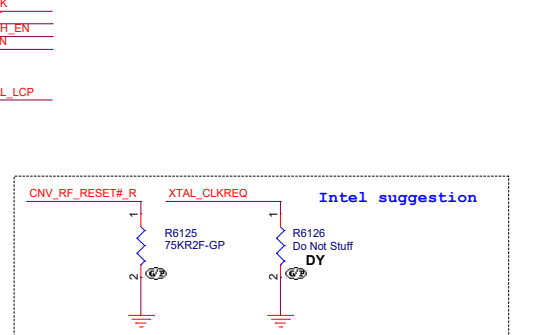
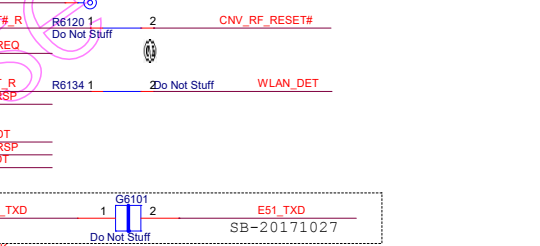
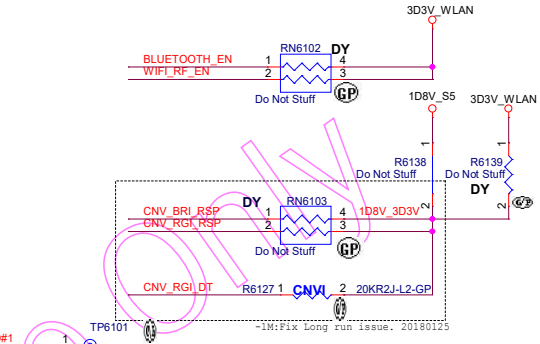
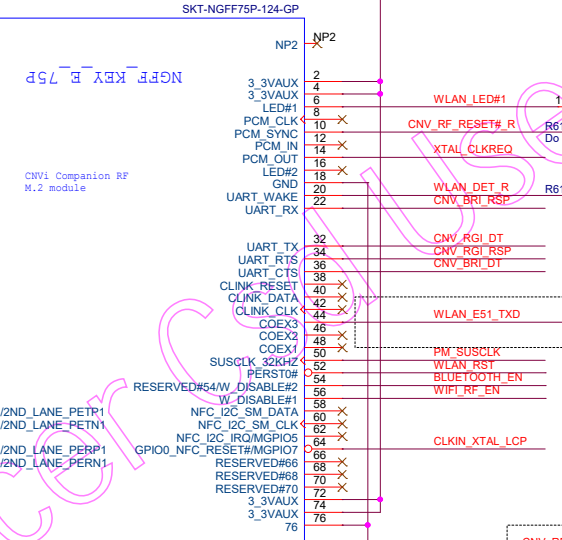
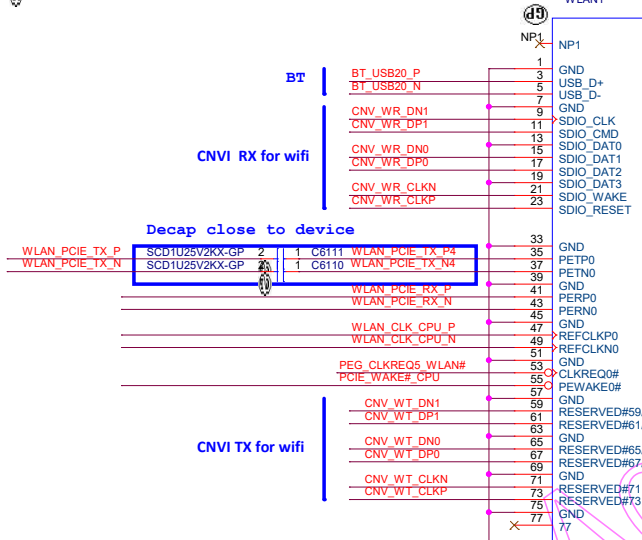
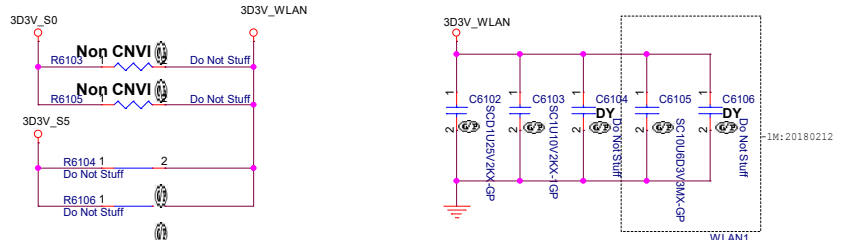
18	BT_USB20_P	<<	
18	BT_USB20_N	<<	

WLAN

18	WLAN_PCIE_TX_P	>>	
18	WLAN_PCIE_TX_N	>>	
18	WLAN_PCIE_RX_P	<<	
18	WLAN_PCIE_RX_N	<<	
18	WLAN_CLK_CPU_P	>>	
18	WLAN_CLK_CPU_N	>>	
18,89	PCIE_WAKE#_CPU	<<	
20	WLAN_DET	<<	
18	WLAN_CLKREQ_CPU_N	<<	

Other

24,89	WIFI_RF_EN	>>	
24,89	BLUETOOTH_EN	>>	
24,68	E51_TXD	>>	
19,89	PM_SUSCLK	>>	
19,24,40,63,68,89,91	PLT_RST#	>>	
17	CLKIN_XTAL_LCP	<<	
24	WLAN_PERST#	>>	
89	WLAN_RST	>>	
89	CNV_RF_RESET#_R	<<	
89	WLAN_DET_R	<<	
89	WLAN_PCIE_TX_P4	<<	
89	WLAN_E51_TXD	<<	
89	PEG_CLKREQ5_WLAN#	<<	



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Size	Document Number
Custom	Sapporo GLK
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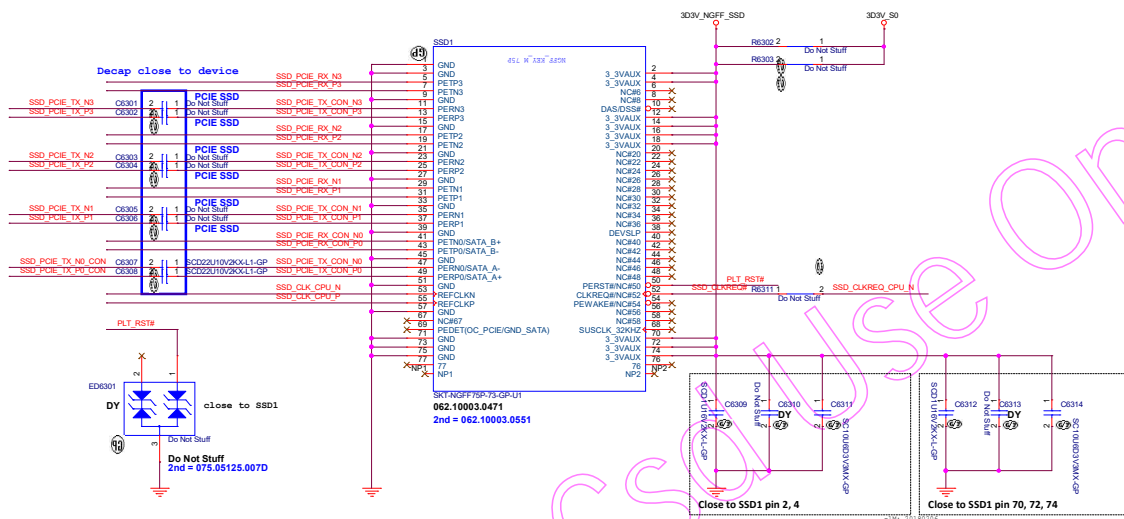
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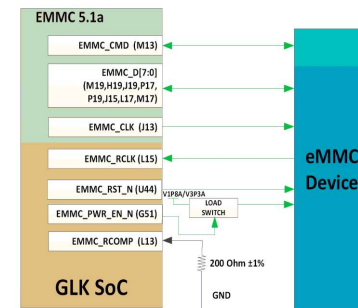
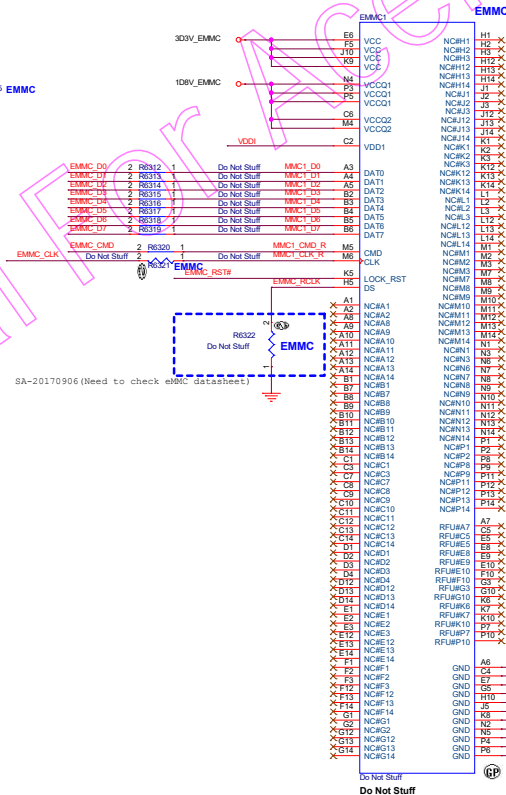
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Title (Reserved)			
Size A4	Document Number Sapporo_GLK		Rev -1M
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TYPE-M NGFF CARD FOR PCIE/SATA SSD



The diagram illustrates the recommended EMMC pin connections for the SA-6L01 module. It includes several individual pin connections and a larger multi-pin connector interface.

- Individual Pin Connections:**
 - R0337:** 3DVS_S0, Do Not Stuff
 - R0338:** 1DVS_S0, Do Not Stuff
 - R0317:** 3DIVV_EMMC
 - R0318:** 1DIVV_EMMC
 - R0319:** EMMC
 - C0315:** VDDI
 - C0316:** EMMC
- Multi-Pin Connector Interface:**
 - 1DIVV_EMMC:** Connected to a series of pins labeled 1R0323 through 1R0332.
 - EMMC_RST#:** Connected to pins 1A0 through 1A9.
 - EMMC_DQ:** Connected to pins 1B0 through 1B9.
 - EMMC_CK:** Connected to pins 1C0 through 1C9.
 - EMMC_L2:** Connected to pins 1D0 through 1D9.
 - EMMC_L1S:** Connected to pins 1E0 through 1E9.
 - EMMC_DS:** Connected to pins 1F0 through 1F9.
 - EMMC_CS:** Connected to pins 1G0 through 1G9.
 - EMMC_D7:** Connected to pins 1H0 through 1H9.
 - EMMC_CMD_X:** Connected to pins 1J0 through 1J9.



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SSID = KBC

Internal KeyBoard Connector

24.06.89 KBC_PWRBTN# <<< _____
24.89 KSJ[0..7] >>> _____
24.89 KSO[0..17] <<< _____
24 KB_BL_PWM >>> _____
24 KB_BL_DET <<< _____
17 CPU_I2C_SCL_P4 <<> _____
17 CPU_I2C_SDA_P4 <<> _____
24 EC_TPCLK <<> _____
24 EC_TPDAT <<> _____
89 CPU_I2C_SDA_TP <<> _____
89 CPU_I2C_SCL_TP <<> _____

89 EC_TP_CLK_C <<> _____
89 EC_TP_DATA_C <<> _____

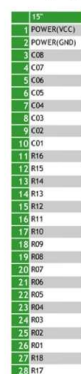
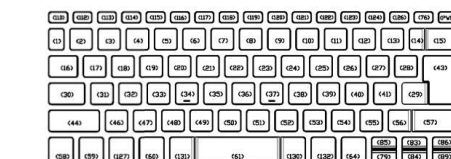
89 TP_IN#_R <<> _____
24.89 TP_FUN_OFF# <<> _____

20 TP_IN#_CPU <<< _____

24 EC_TP_IN# <<< _____

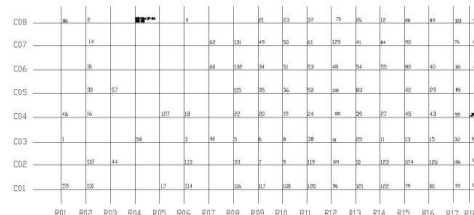
24 PTP_PWR_EN >>> _____

89 KB_LED_PWM_R <<< _____
89 KB_BL_DET_R <<< _____

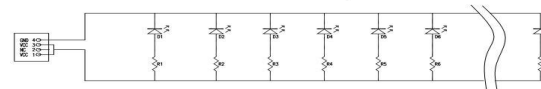


PIN 1
VCC

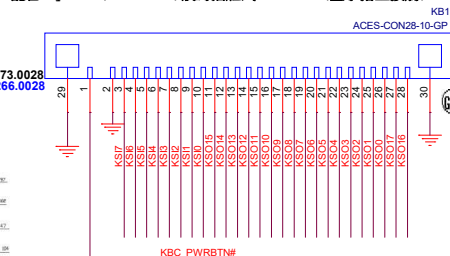
PIN2 GND



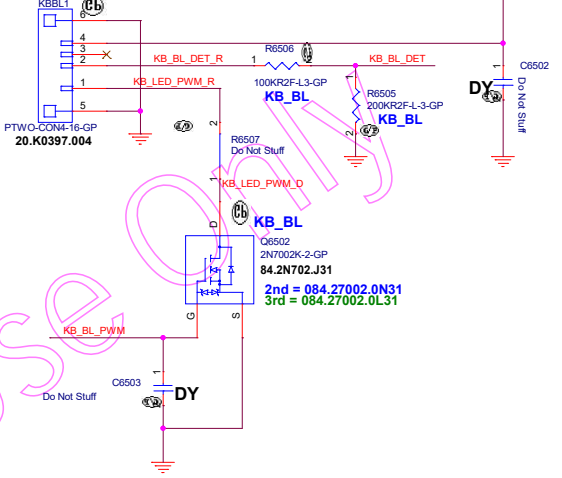
LED	Model : SMD 0402 QTY : 10 pcs Value : 68 ohm Tolerance : +/- 1%
RESISTANCE	Model : SMD 0402 QTY : 10 pcs Value : 68 ohm Tolerance : +/- 1%



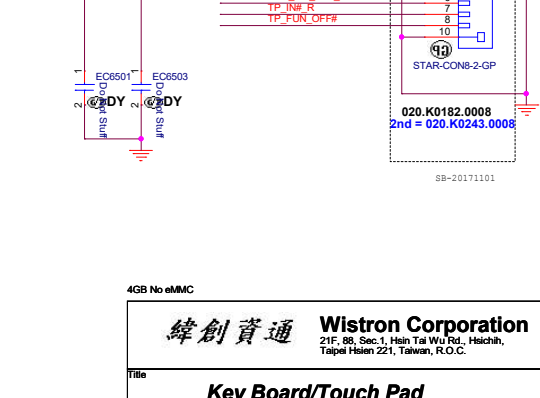
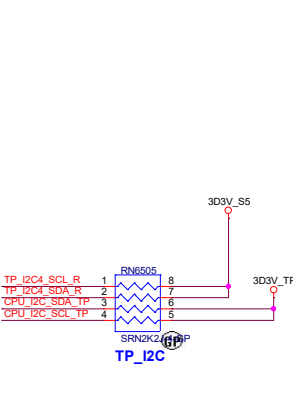
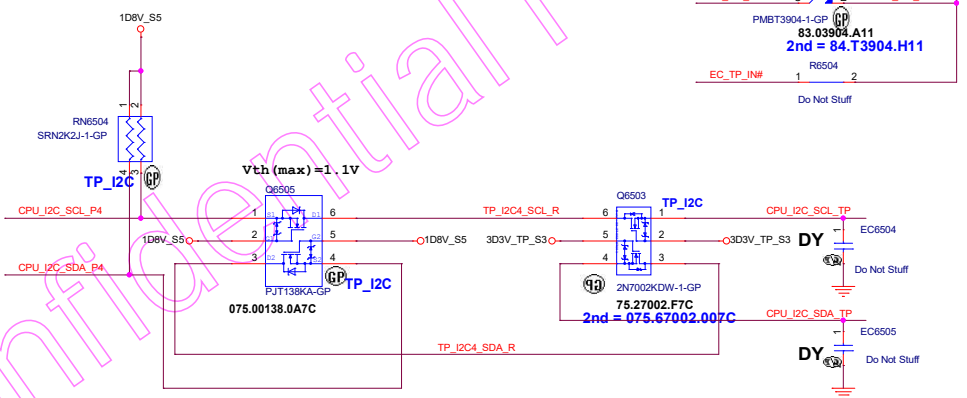
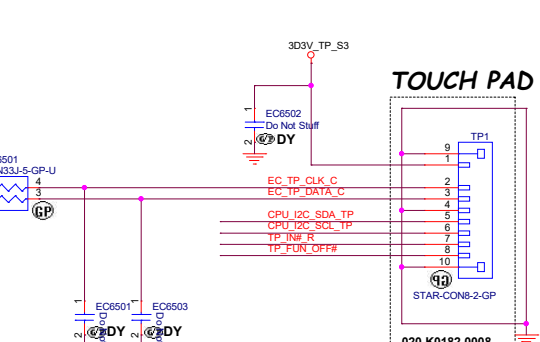
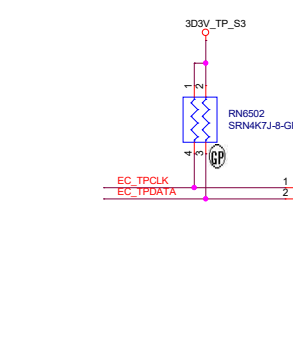
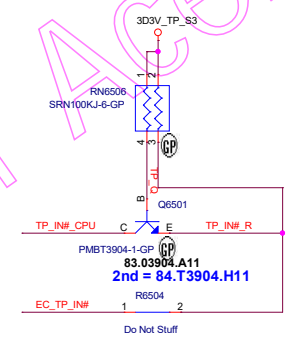
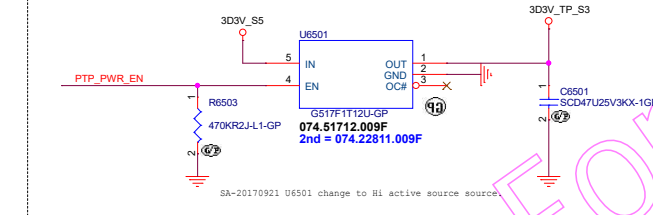
SA-20170928 Change KB1 source
配合Keyboard (CARBON UP) 改為抽屜式 connector (金手指上接觸)



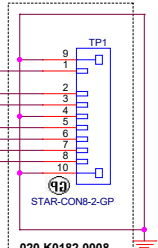
KB_BL



High Active 2A



TOUCH PAD



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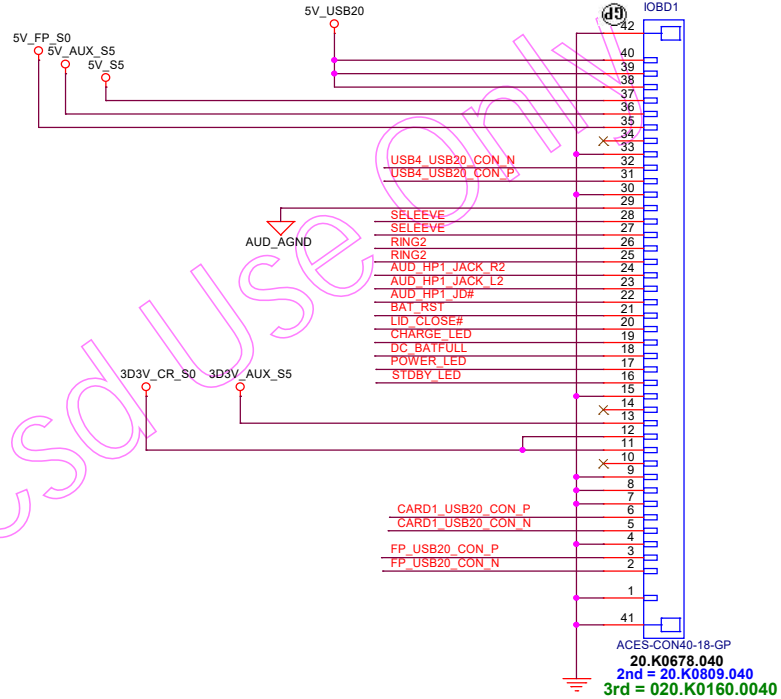
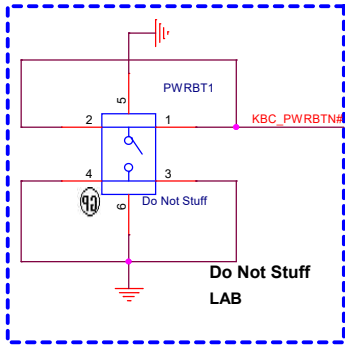
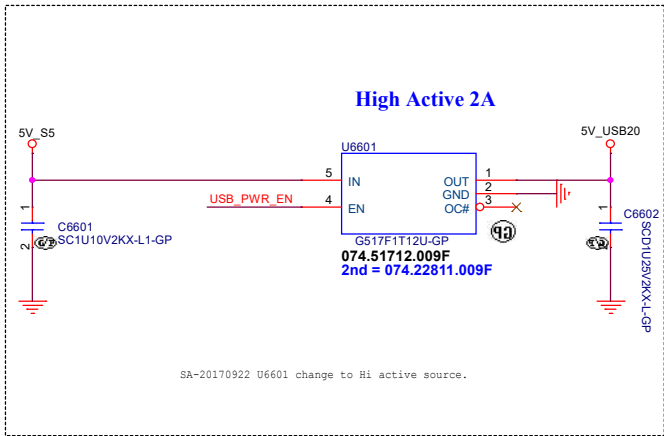
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

Key Board/Touch Pad
Sapporo GLK
Date: Tuesday, February 13, 2018 Sheet 65 of 106

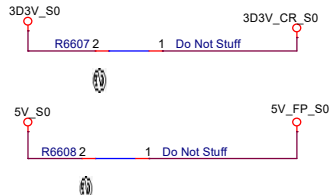
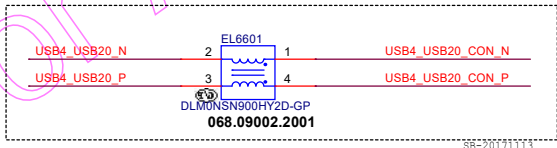
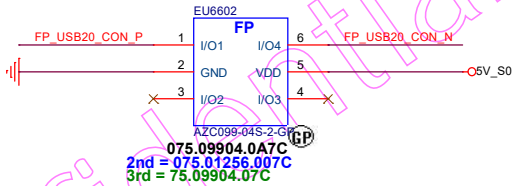
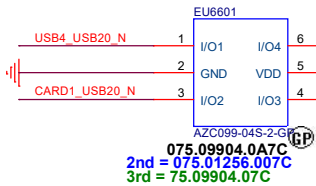
IO CONN

SSID = User.Interface

- 24,66,89 STDBY_LED >>>
- 24,66,89 POWER_LED >>>
- 24,66,89 CHARGE_LED >>>
- 24,66,89 DC_BATFULL >>>
- 24,89 LID_CLOSE# <<<
- 18 USB4_USB20_N <<<
- 18 USB4_USB20_P <<<
- 18 CARD1_USB20_P <<<
- 18 CARD1_USB20_N <<<
- 43,89 BAT_RST <<<
- 24,65,89 KBC_PWRBTN# <<<
- 24,35 USB_PWR_EN >>>
- 27,66,89 RING2 >>>
- 27,66,89 RING2 >>>
- 27,66,89 SELEEVE >>>
- 27,66,89 SELEEVE >>>
- 27 AUD_HP1_JACK_R2 <<<
- 27,89 AUD_HP1_JACK_L2 <<<
- 27,89 AUD_HP1_JD# <<<
- 38 FP_USB20_P <<<
- 38 FP_USB20_N <<<
- 24,66,89 STDBY_LED <<<
- 24,66,89 POWER_LED <<<
- 24,66,89 CHARGE_LED <<<
- 24,66,89 DC_BATFULL <<<
- 89 USB4_USB20_CON_P <<<
- 89 USB4_USB20_CON_N <<<
- 89 CARD1_USB20_CON_P <<<
- 89 CARD1_USB20_CON_N <<<
- 89 FP_USB20_CON_N <<<
- 89 FP_USB20_CON_P <<<



Close connector

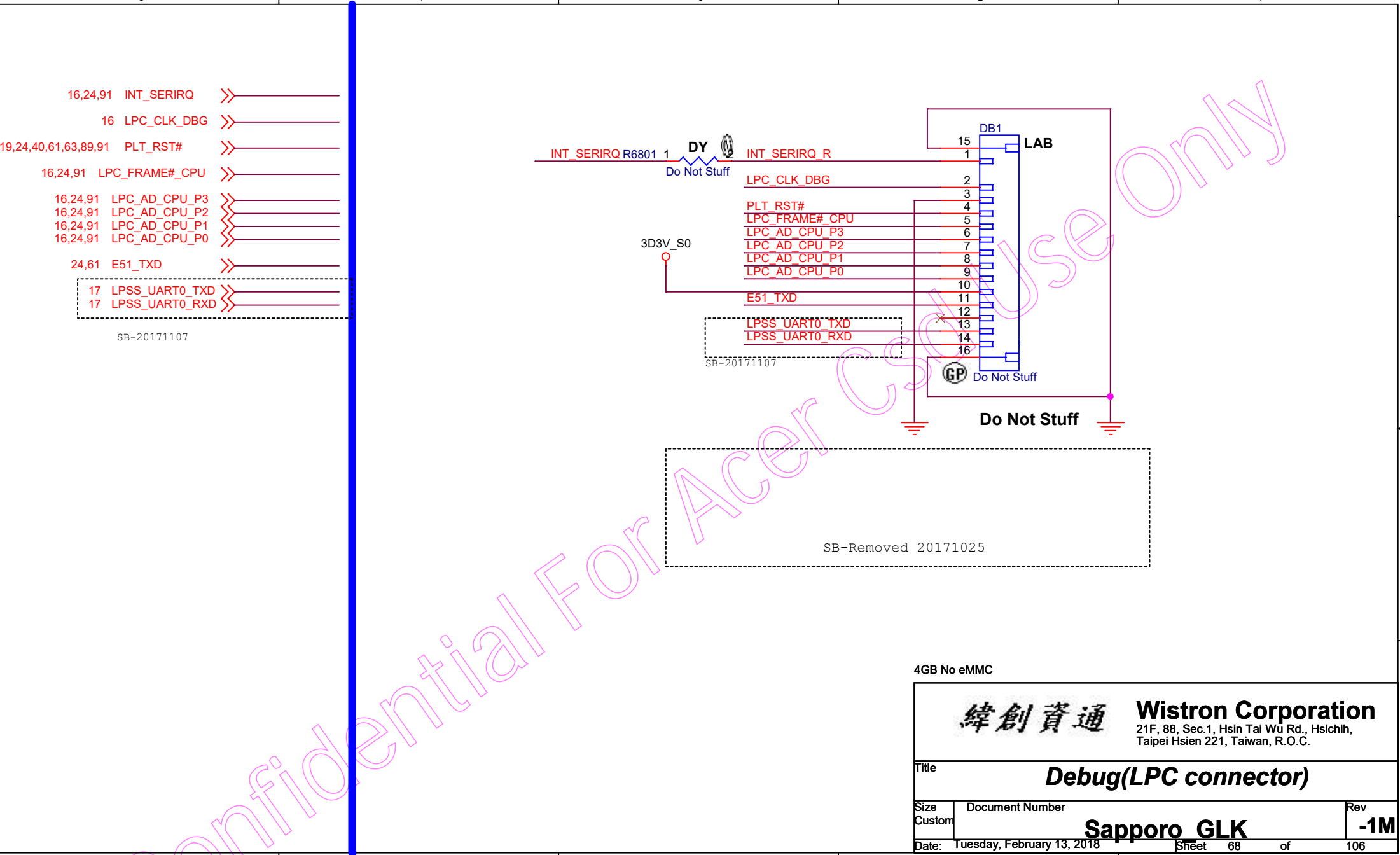


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Title

G Sensor (Reserved)

Size
A4

Document Number

Sapporo_GLK

Rev
-1M

Date: Tuesday, February 13, 2018

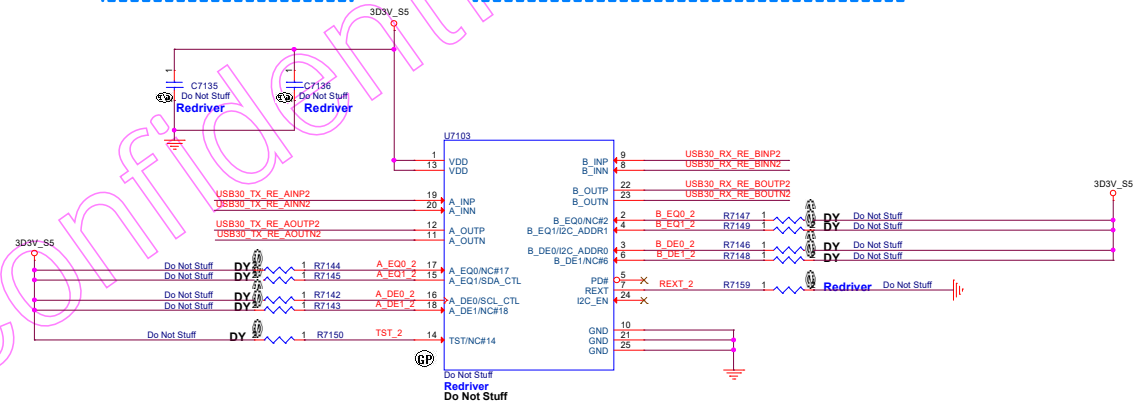
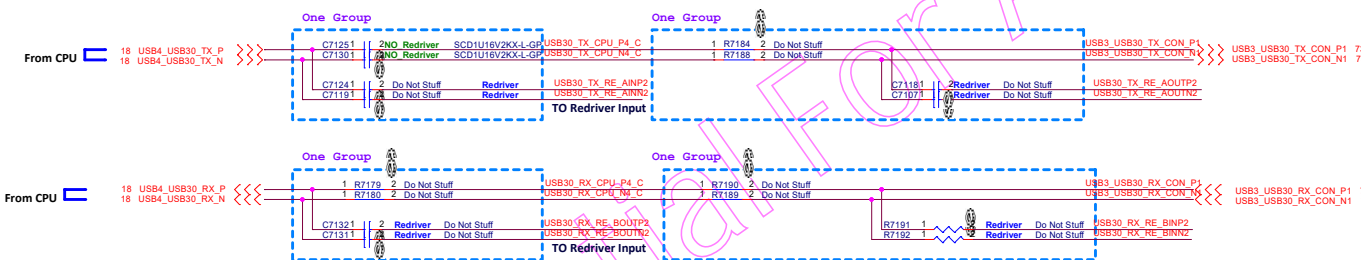
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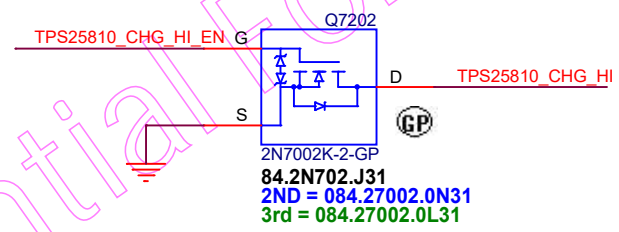
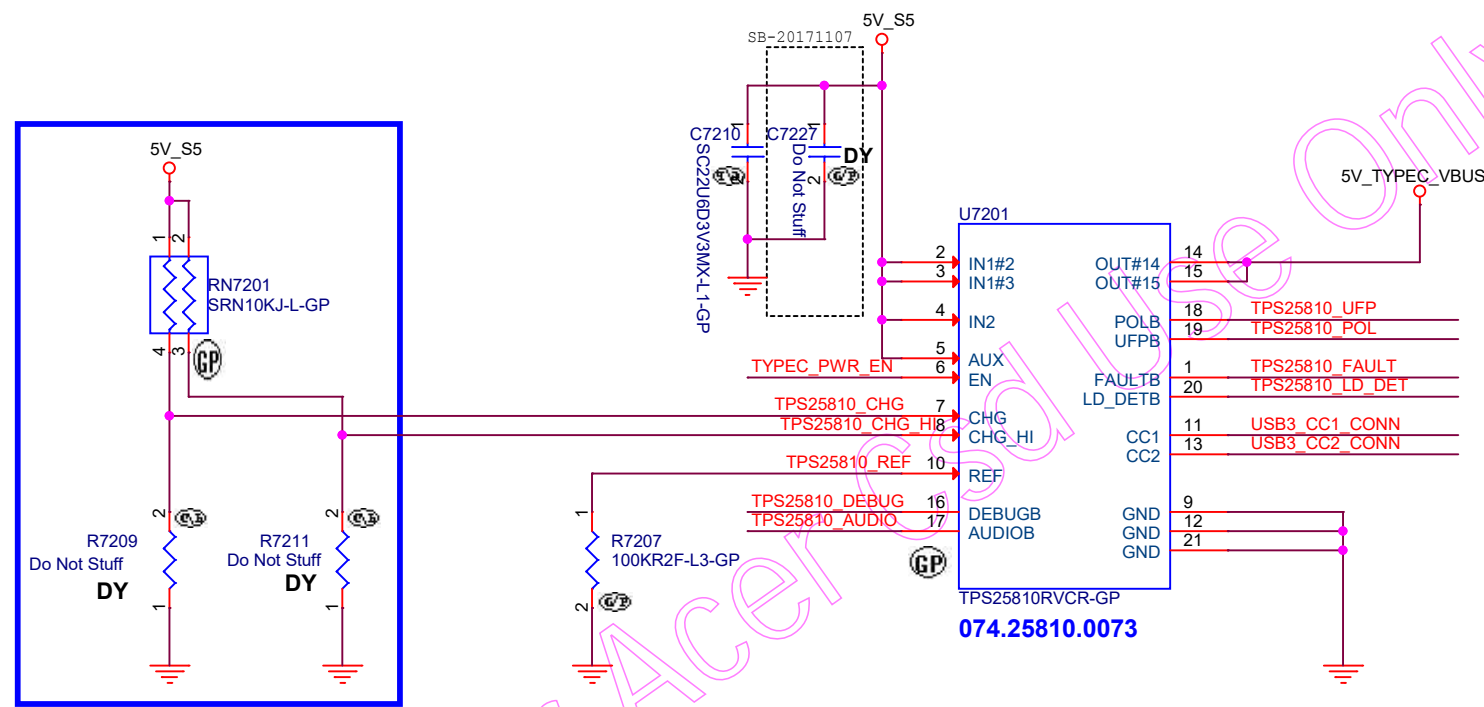
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24 TYPEC_PWR_EN >>>
24 TPS25810_CHG_HI_EN >>>
73,89 USB3_CC1_CONN <<<
73,89 USB3_CC2_CONN <<<



- These nets are just for debug use
- | | | | |
|-----------------|---|--------|--------------|
| TPS25810_FAULT | 1 | TP7201 | Do Not Stuff |
| TPS25810_LD_DET | 1 | TP7202 | Do Not Stuff |
| TPS25810_UFP | 1 | TP7203 | Do Not Stuff |
| TPS25810_POL | 1 | TP7204 | Do Not Stuff |
| TPS25810_AUDIO | 1 | TP7205 | Do Not Stuff |
| TPS25810_DEBUG | 1 | TP7206 | Do Not Stuff |

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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Type C CC Logic

Size A4

Document Number

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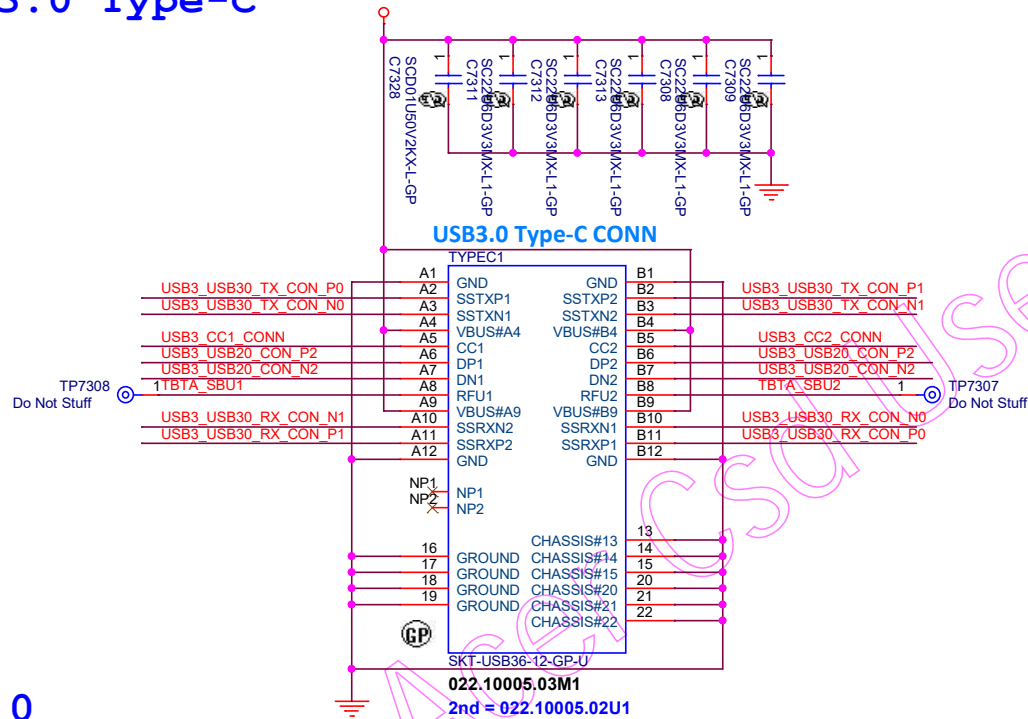
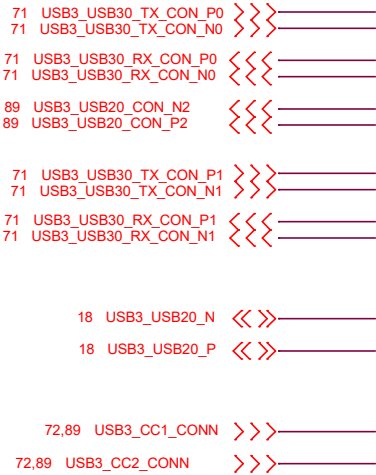
Rev -1M

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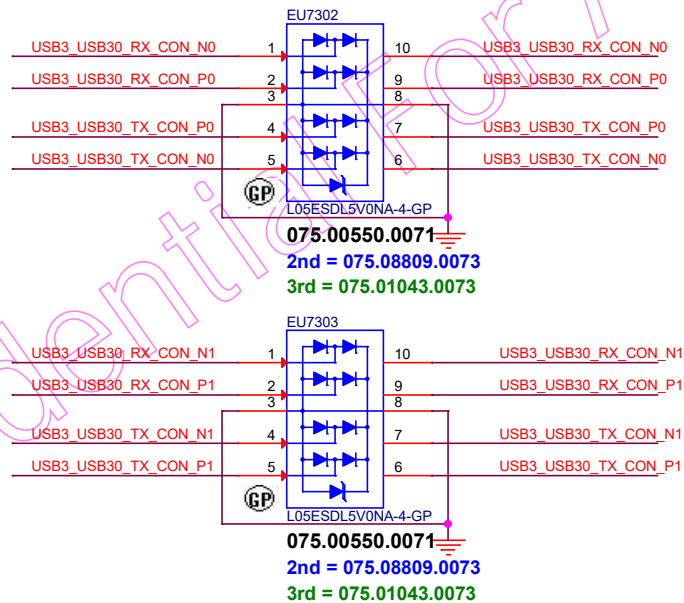
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USB3.0 Type-C

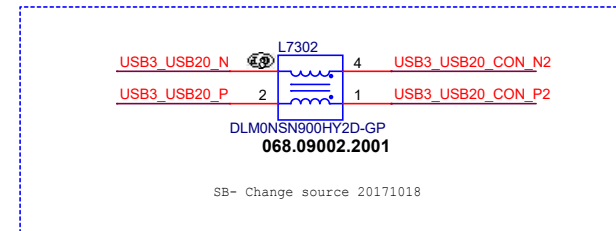
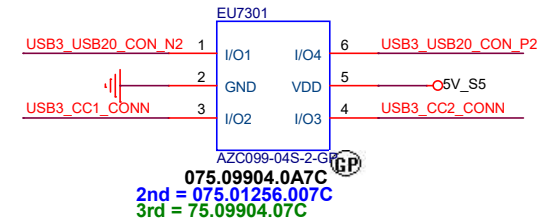
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ESD 3.0



ESD 2.0 & CC



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Title EXT IO(TYPEC_TPS25810RVCR-GP)	
Size Custom Document Number Sapporo GLK	Rev -1M
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Title

GPU (1/5) PEG

Size

A4

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Title GPU (2/5) DIGITAL		
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Title GPU (3/5) VRAM			
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Title GPU (4/5) GPIO			
Size A4	Document Number Sapporo_GLK		Rev -1M
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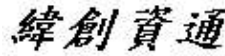
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Title GPU (5/5) PWR/GND			
Size A4	Document Number Sapporo_GLK		Rev -1M
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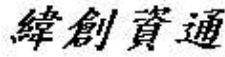
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Title VRAM3,4 (2/4)			
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Title

VRAM5,6 (3/4)

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Title VRAM7,8 (4/4)		
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Title DISCRETE VGAPOWER		
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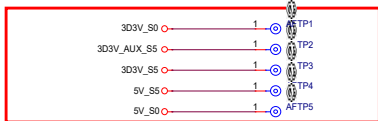
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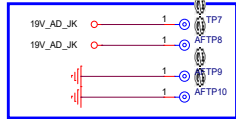
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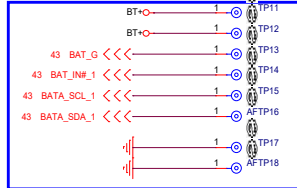
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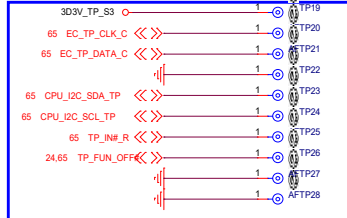
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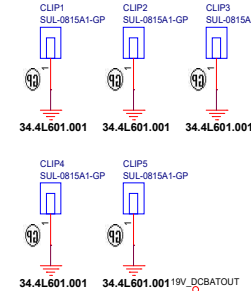
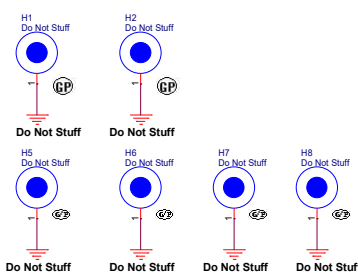
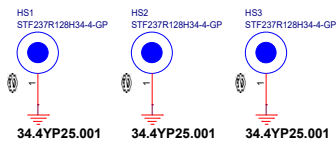
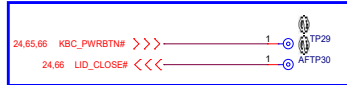
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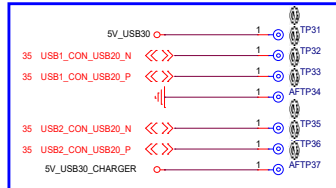
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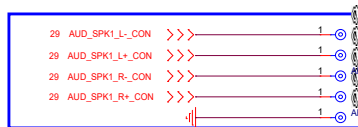
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USB3.0



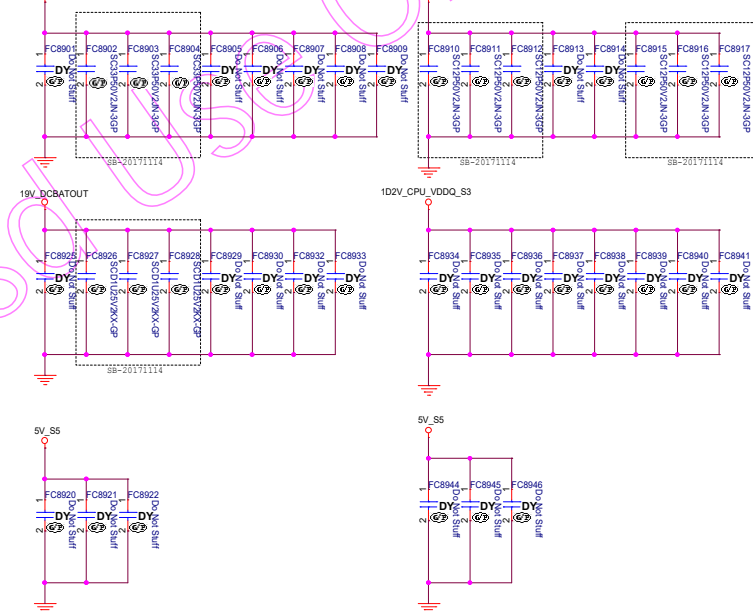
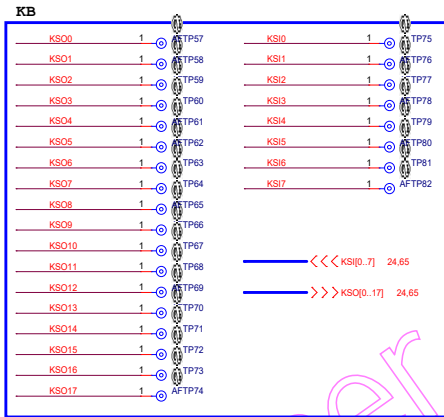
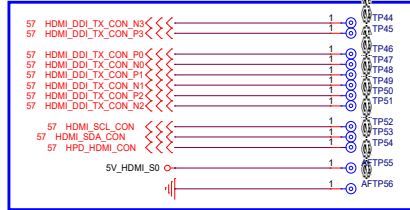
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WLAN

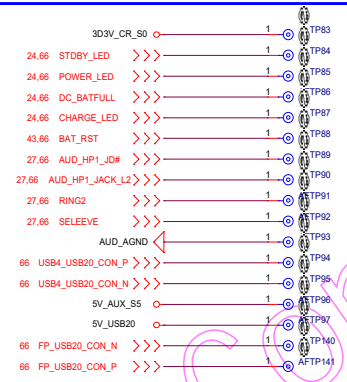


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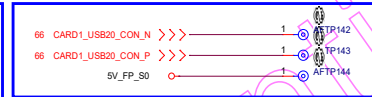


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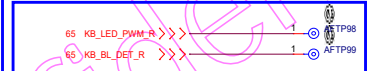
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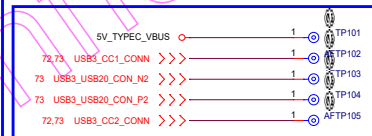
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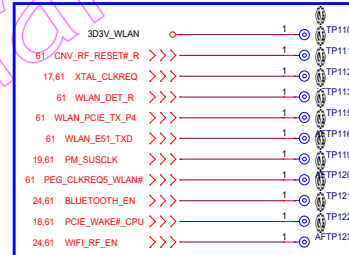
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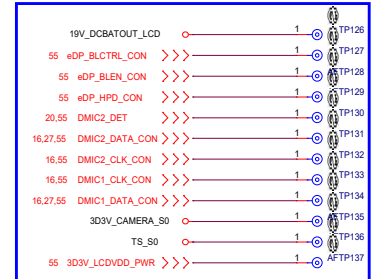
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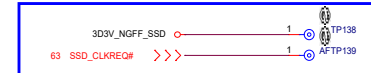
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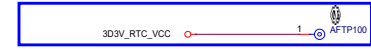
LCD1



SSD1



RTC1



SB-Add AFTP 20171106

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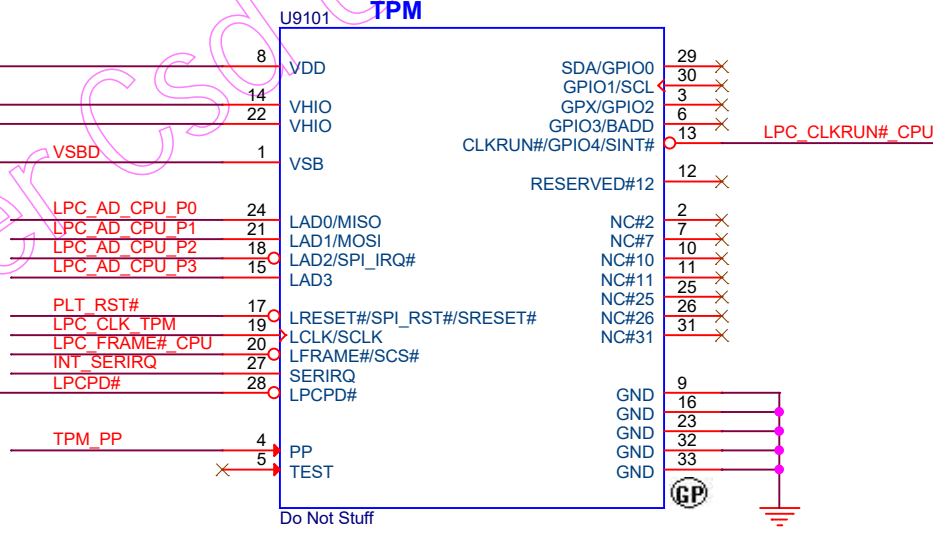
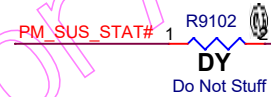
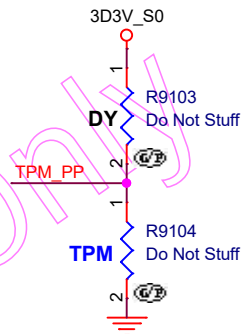
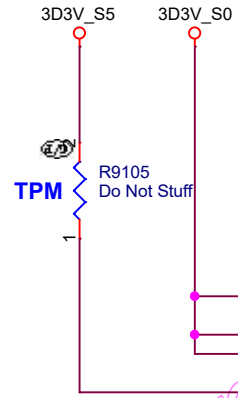
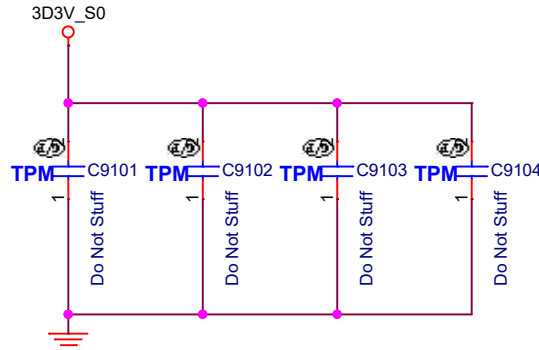
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9,24,40,61,63,68,89 PLT_RST# <<<
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16,24 LPC_CLKRUN#_CPU <<<
19 PM_SUS_STAT# >>>



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G3 to S5/S4

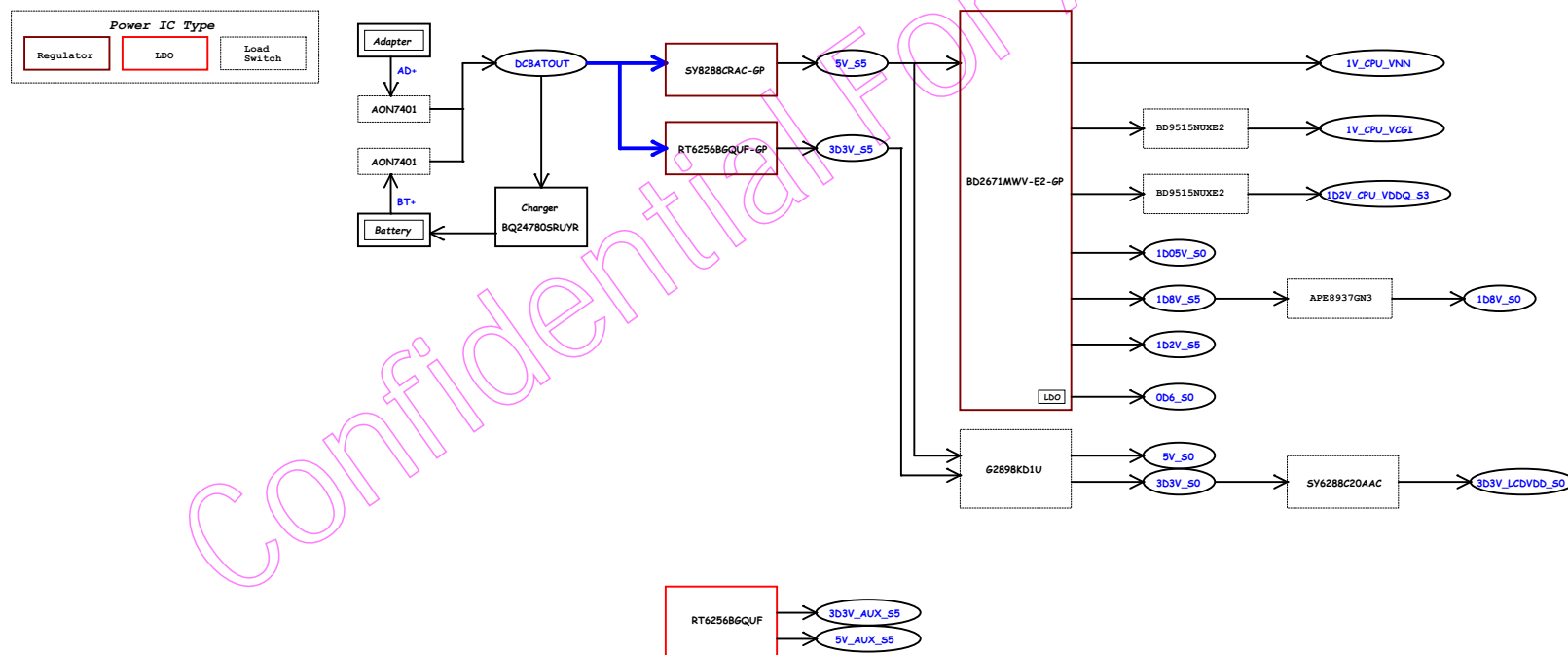
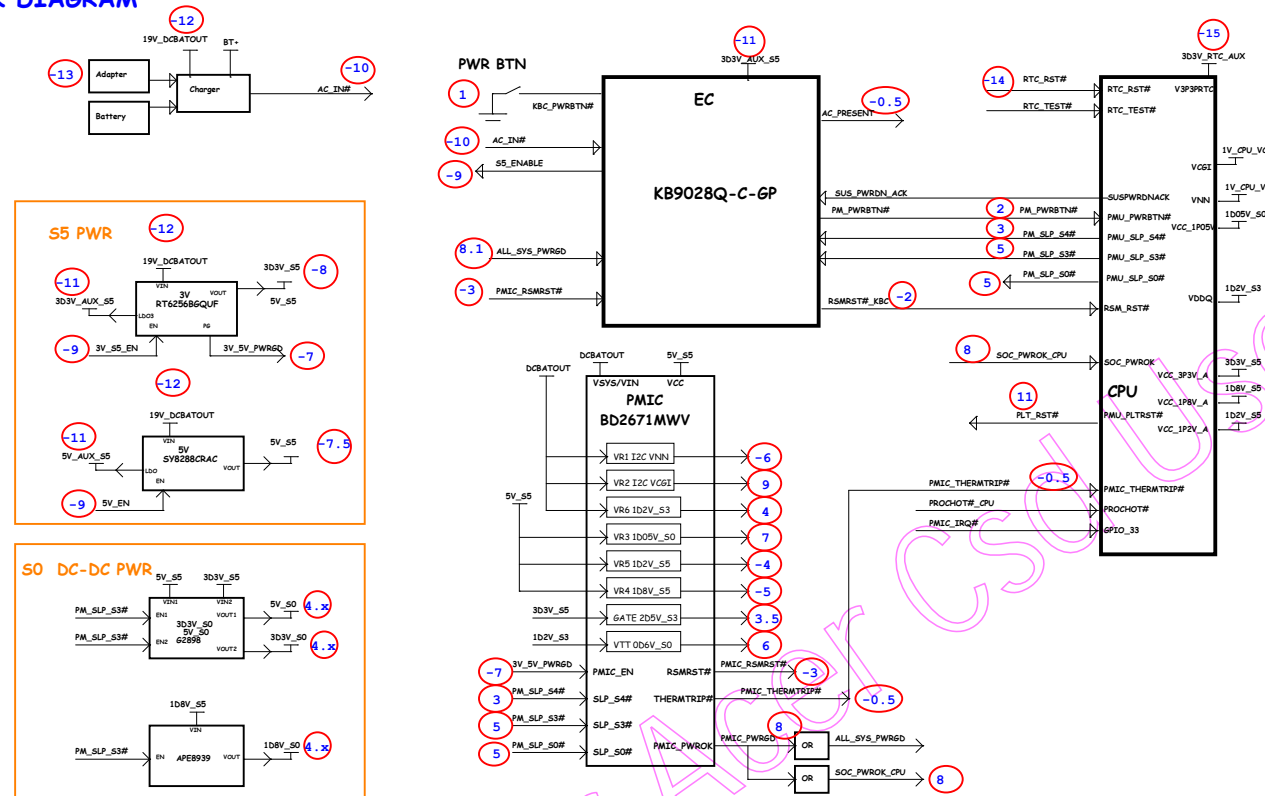


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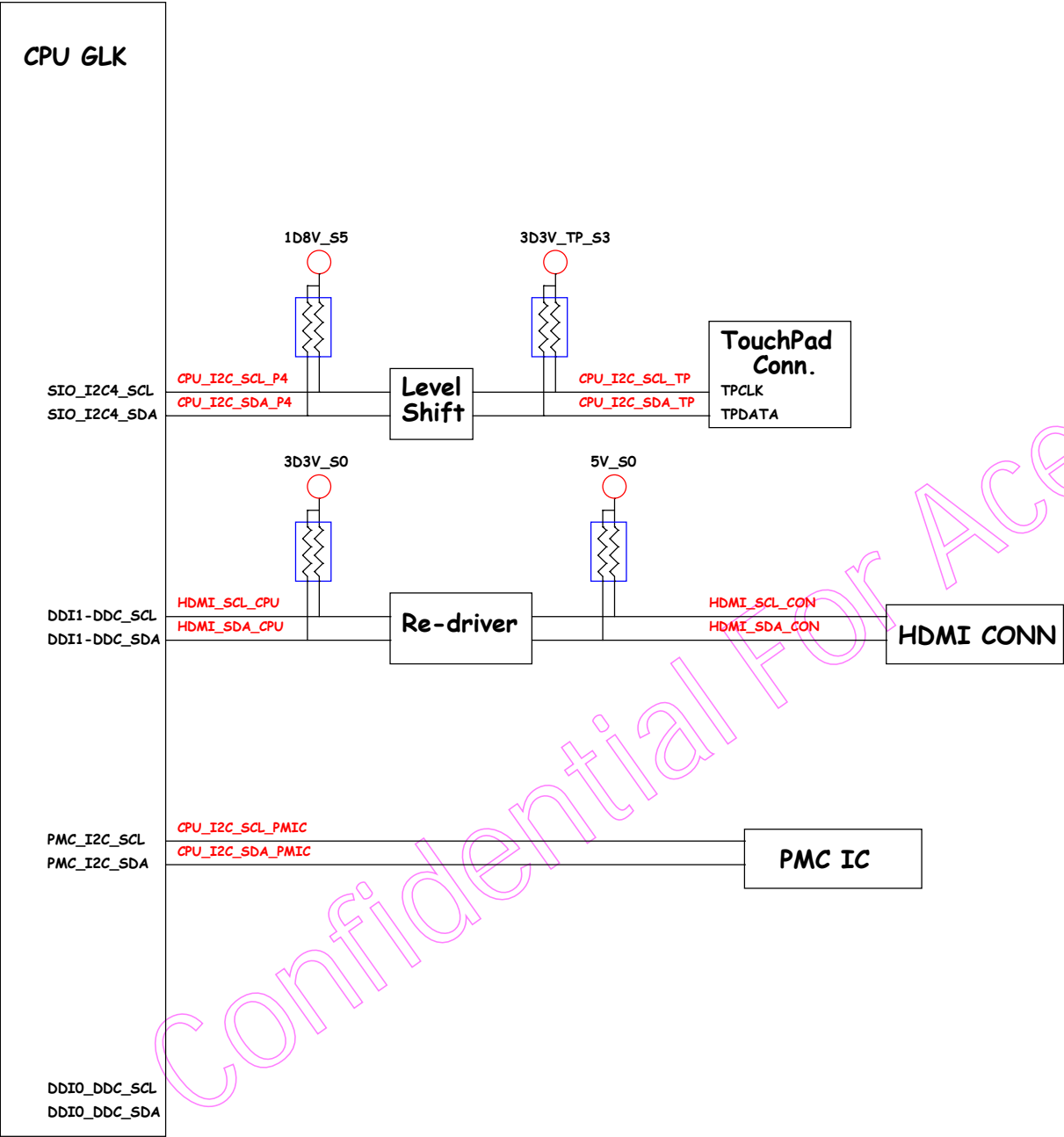


Gemini Lake G3 Cold Boot Power-Up

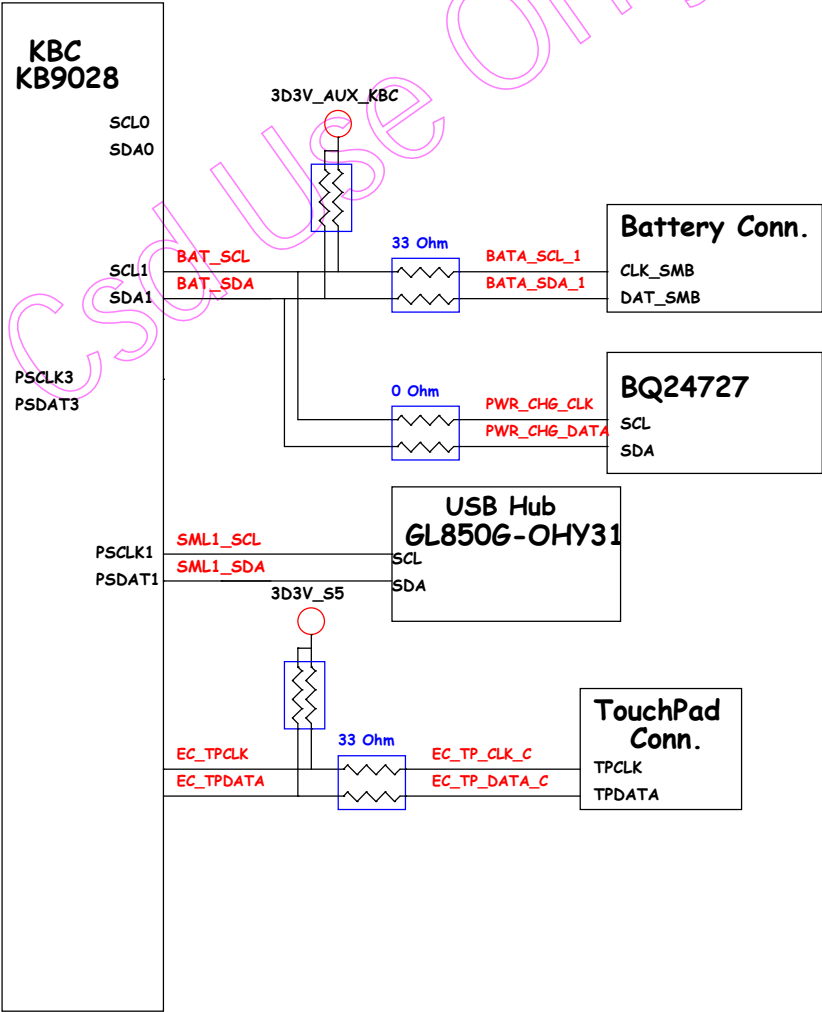
Gemini LAKE SEQUENCE & BLOCK DIAGRAM



PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title **THERMAL/AUDIO BLOCK DIAGRAM**

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